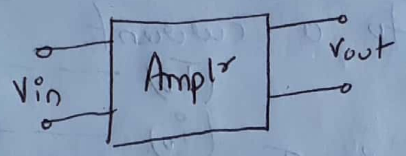
JFET amplifiers

Module 5.1 : Understanding concept of amplification with reference to transfer / o/p characteristics of JFET

- Amplifier requirements :

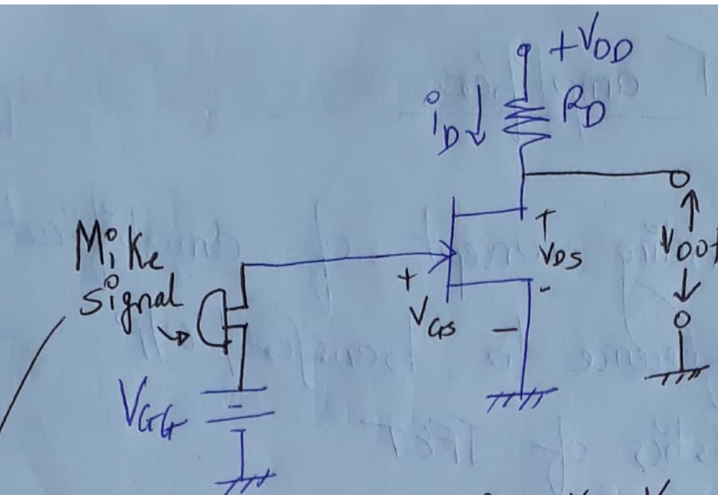


1) Gain should be high
eg voltage gain of a voltage ampl^r → high
2) I/p impedance
3) o/p impedance
4) Linearity (o/p should be Linear w.r.t I/p)

- JFET as a device should amplify → small time-varying signals.

This condition must be satisfied for JFET amplifier to be $\boxed{\text{Linear}}$

- Next, we need to superimpose small AC s/g with DC ? why DC biasing is required → So that JFET wakes up & works in proper mode i.e saturation → so that it is used as amplifier.

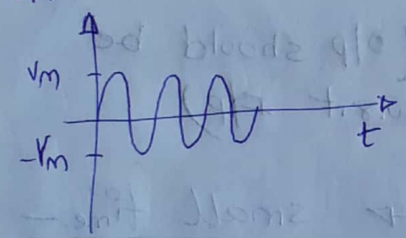


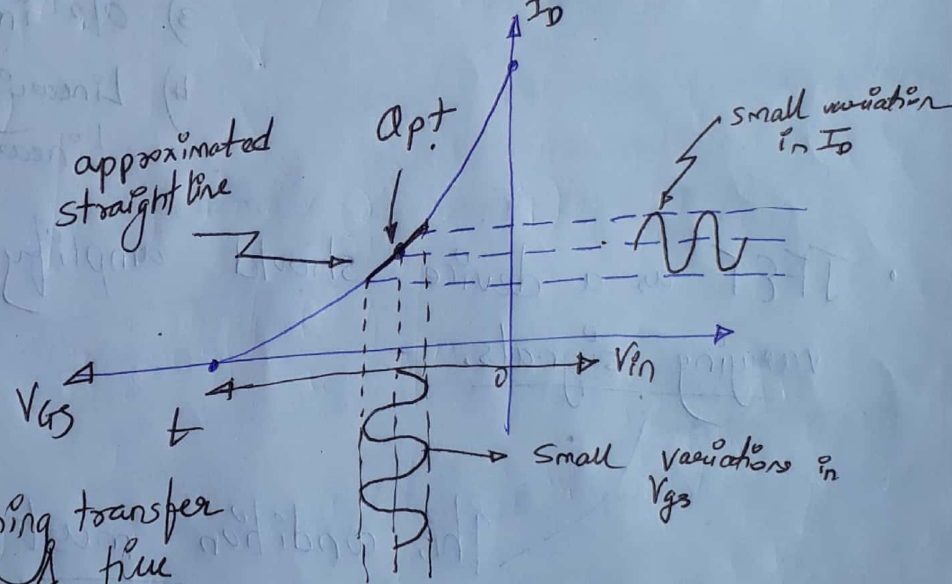
It acts a small time-varying I/P V_{in} ($V_{mike} \approx V_m \sin \omega t$)

→ JFET acts as : voltage - dependent current source

→ "converts" a voltage (V_{GS}) or (V_{gs}) to a current (I_D) — DC quantity (i_D) — AC quantity

→ It's a V-I converter ie Transconductor

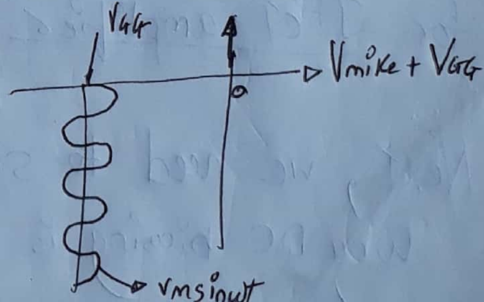




→ Here, the idea is to consider small segment of exponenti. curve to be Linear

Combining transfer curve & time response.

ie



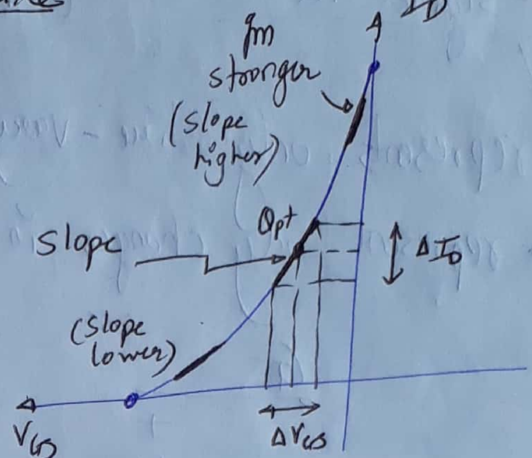
→ So, our I/p (limit) should be within this Linear segment → Hence, called as small sig

• Concept of transconductance

From graph,

$$\boxed{g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{opt}}$$

slope of I_D vs V_{GS} characteristics



Unit: $\frac{1}{\Omega}$ or $\frac{mA}{V}$

ie $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ $\Rightarrow$ $\boxed{\Delta I_D = g_m \Delta V_{GS}}$ --- Powerful Concept

ΔI_D → small changes in I_D

g_m → slope → a constant

ΔV_{GS} → small changes in V_{GS}

It suggest that gate to source voltage controls the drain to source current in a JFET

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

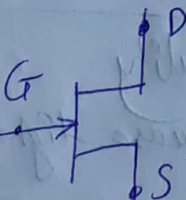
$$\frac{dI_D}{dV_{GS}} = -\frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$\boxed{g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)}$$ --- Mathematically

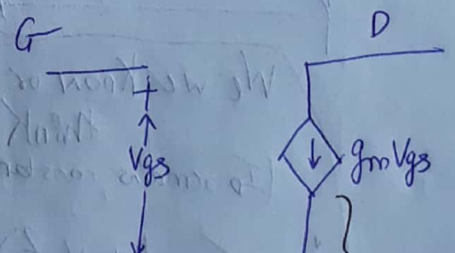
$$g_{mo} = \frac{2I_{DSS}}{|V_P|} \quad \text{ie} \quad \boxed{g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)}$$

$V_{gs} \simeq \Delta V_{GS}$ → time-varying

Now, we are ready to draw small-signal model of JFET



$\Rightarrow$



→ Gate to source is open ckt!

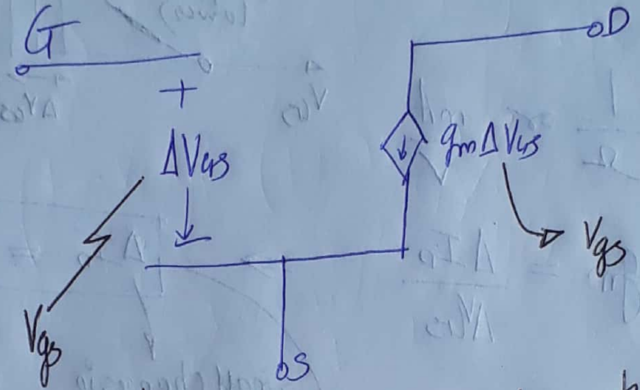
{ I/P impedance of a JFET is high, hence $I_G \simeq 0$, since G-S junction of a JFET is always reverse-bias }

→ represents change in I_D

ie $\boxed{\Delta I_D \simeq g_m \Delta V_{GS}}$

Small-signal model → (represents only time-varying quantities) 04

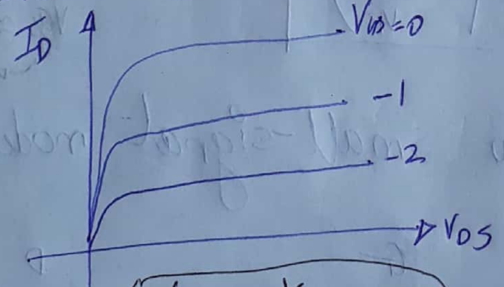
- represents only time-varying components
- represent only changes in parameters (voltage V_{gs}, current i_D)

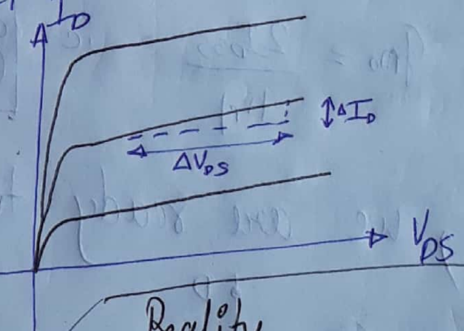


Small-slg model of JFET suggests that the drain current fluctuations (ΔI_D) is equal to V_{GS} fluctuation (ΔV_{GS}) times the slope (g_m)

- **Small-slg o/p resistance/impedance (r_o or r_d):**

Let's consider o/p characteristics of JFET





We we know or think
(I_D remains constant)

$$i_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Reality
(I_D increase slightly with V_{DS})

$$i_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 (1 + \lambda V_{DS})$$

λ - channel length modulation parameter

Scanned by CamScanner

From graph, $(I_D - V_{DS})$

$$\text{Slope} = \frac{\Delta I_D}{\Delta V_{DS}}$$

$$\boxed{\frac{1}{\text{slope}} = \frac{\Delta V_{DS}}{\Delta I_D} = r_o \text{ or } r_d}$$

small-slg o/p resistance of a JFET biased in saturation region.

ie $i_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 (1 + \lambda V_{DS})$

$$\frac{di_D}{dV_{DS}} = \underbrace{\lambda I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

$$\frac{di_D}{dV_{DS}} = \lambda I_{DQ}$$

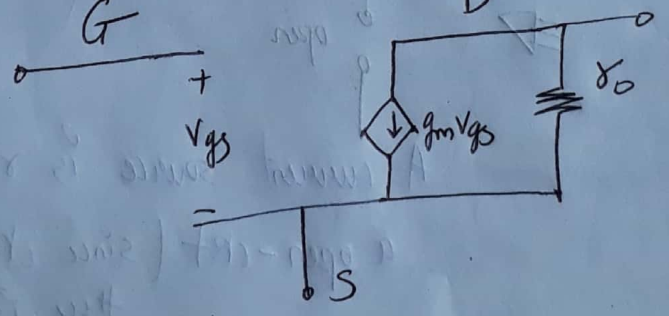
ie $\frac{dV_{DS}}{di_D} = \frac{1}{\lambda I_{DQ}}$ ie $\boxed{r_o \text{ or } r_d = \frac{1}{\lambda I_{DQ}}}$

small-slg o/p resistance

We need to include <u>this</u> in small-slg model, (We connect r_d betn D&S)

Complete small-slg model of n-JFET ----- Congratulation

We have small-slg model of JFET finally!

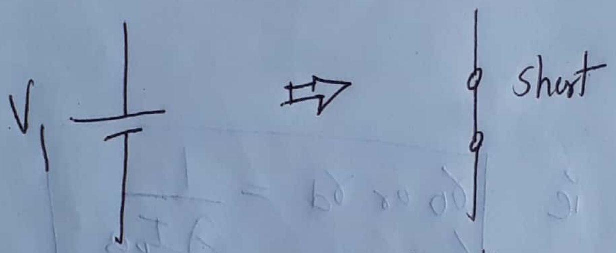


→ Small-signal model of Constant sources:

(they doesn't change with time)

(ie their variation in time is zero)

1) Constant voltage source



A voltage source (DC) is represented by a short (since changes in voltage with time is zero)

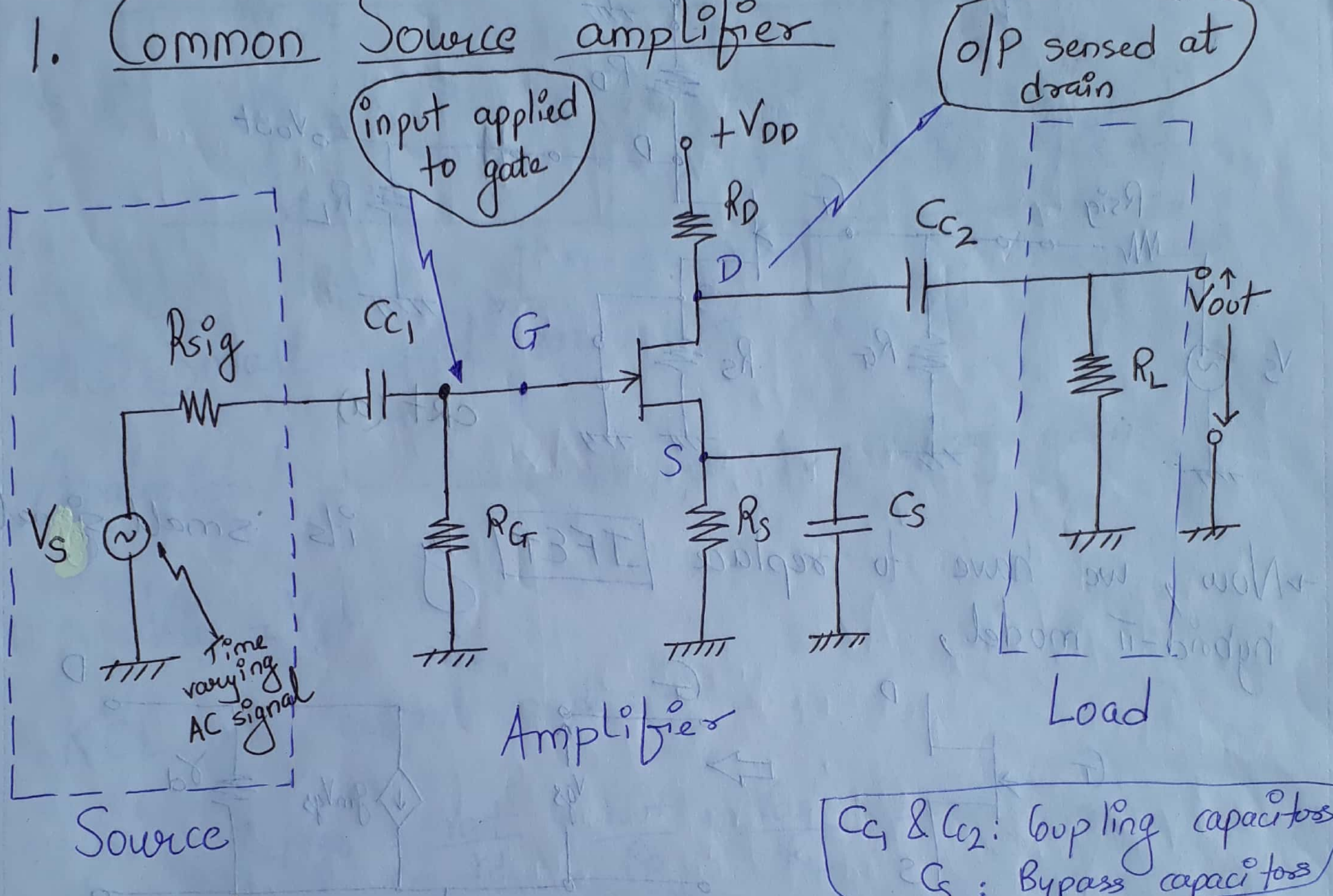
2) Constant current source

A current source is represented by a open-ckt (since changes in current with time is zero)

AC Analysis of JFET amplifier :-

01
11/10/19

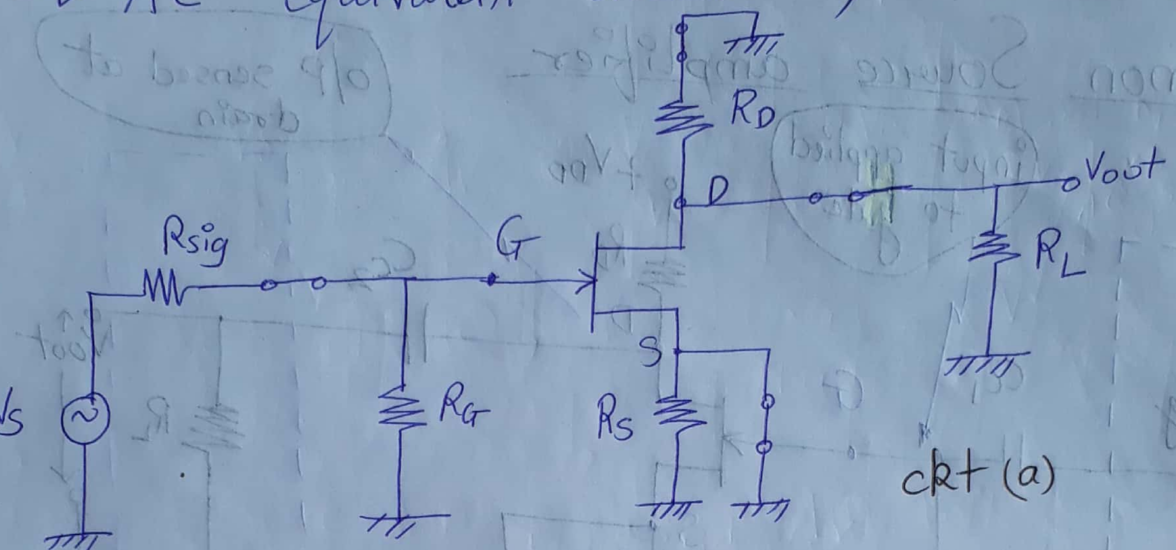
1. Common Source amplifier



Observations :-

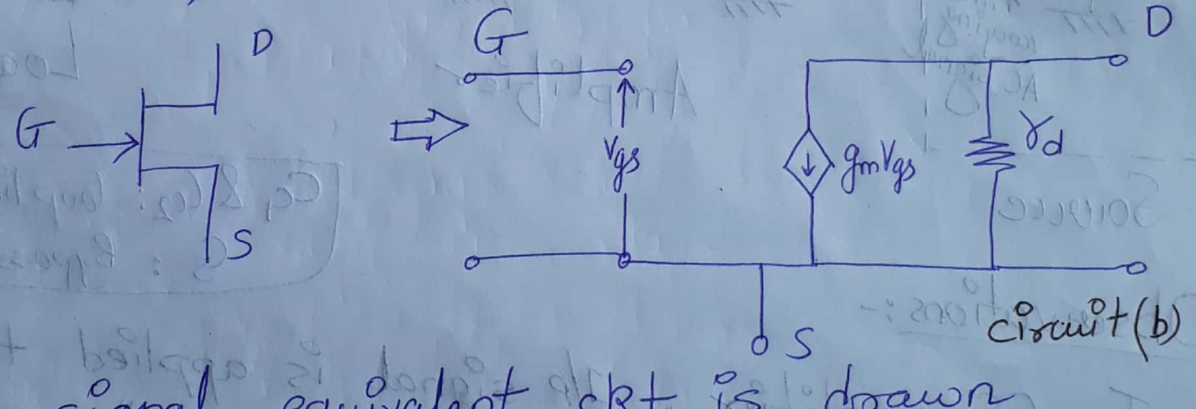
1. In CS amplifier, I/P signal is applied to "gate" terminal and o/p is sensed at the "drain" terminal.
2. For AC analysis, all the capacitors are replaced by a short circuit → as the capacitive impedances $\left(X_C = \frac{1}{2\pi f C}\right)$ are very low at mid-frequencies
3. DC supply is also replaced by a short circuit for small signal (AC) analysis

→ AC equivalent circuit is,



ckt (a)

→ Now, we have to replace $\boxed{JFET}$ by its small-signal hybrid-π model,

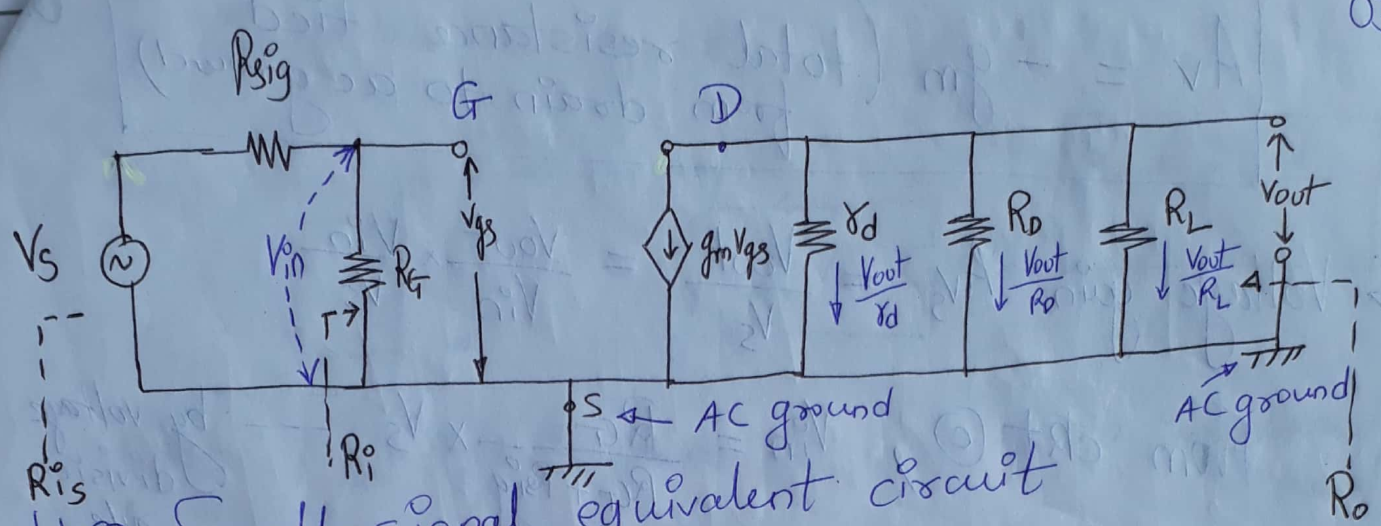


circuit (b)

→ Small-signal equivalent ckt is drawn next by combining ckt (a) & ckt (b)

Note : V_S → I/P time varying signal

V_{out} → O/P time varying signal



ckt ©: Small-signal equivalent circuit

<u>Analysis:-</u> ------→ Find A_v : Voltage gain

- $V_{in} = V_{gs}$

KCL at output node :-

$$g_m V_{gs} + \frac{V_{out}}{r_d} + \frac{V_{out}}{R_D} + \frac{V_{out}}{R_L} = 0$$

$$\text{ie } g_m V_{in} + V_{out}\left(\frac{1}{r_d} + \frac{1}{R_D} + \frac{1}{R_L}\right) = 0$$

$$g_m V_{in} = -V_{out} / (r_d \parallel R_D \parallel R_L)$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = -g_m (r_d \parallel R_D \parallel R_L)$$

$$\boxed{A_v = -g_m (r_d \parallel R_D \parallel R_L)} \quad — ①$$

-ve sign indicates i/p & o/p signals are opposite in phase

$$\boxed{A_v = -g_m\,(\text{total resistance tied from drain to ac ground})}$$

→ Voltage gain $A_{v_s} = \dfrac{V_{out}}{V_s} = \dfrac{V_{out}}{V_{in}} \times \dfrac{V_{in}}{V_s}$

From ckt ⓒ, $V_{in} = \dfrac{R_G}{R_G + R_{sig}} \times V_s$ --- by voltage division rule

ie $\dfrac{V_{in}}{V_s} = \dfrac{R_G}{R_G + R_{sig}}$

$$\therefore \boxed{A_{v_s} = A_v \times \left(\frac{R_G}{R_G + R_{sig}}\right)}$$

Voltage gain including signal source resistance R_{sig}

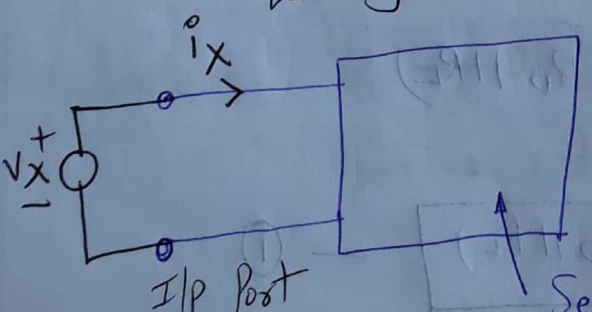
Quick refresher !

- Concept of port impedance :-

Looking at I/p of ckt

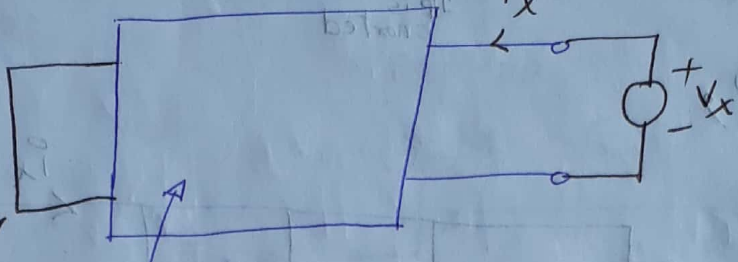
$$\boxed{R_{in} = \frac{V_x}{i_x}}$$

I/p impedance/resistance of a ckt



Set all independent sources to zero

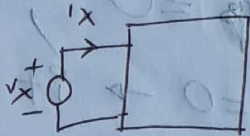
Looking at the o/p of ckt



$$\boxed{R_{out} = \frac{v_x}{i_x}}$$

o/p impedance/resistance

Input and o/p impedances :-



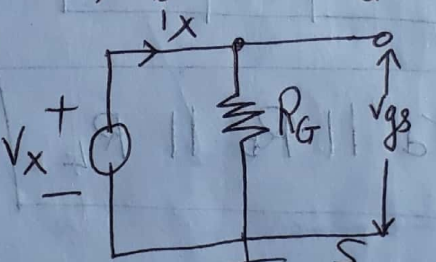
$$R_i = \frac{v_x}{i_x}$$

a) Input impedance :-

In ckt ⓒ, gate & source terminal are open-circuited since gate current in JFET is v.v small ($I_G \simeq 0$)

→ ckt reduces to,

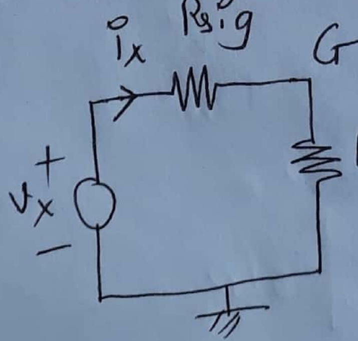
i) without R_{sig}



$$R_i = \frac{v_x}{i_x}$$

$$\boxed{R_i = R_G}$$

ii) with R_{sig}

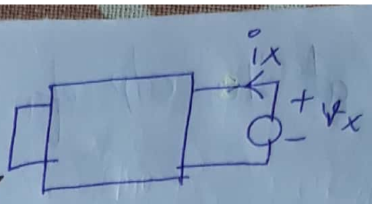


$$R_i = \frac{v_x}{i_x}$$

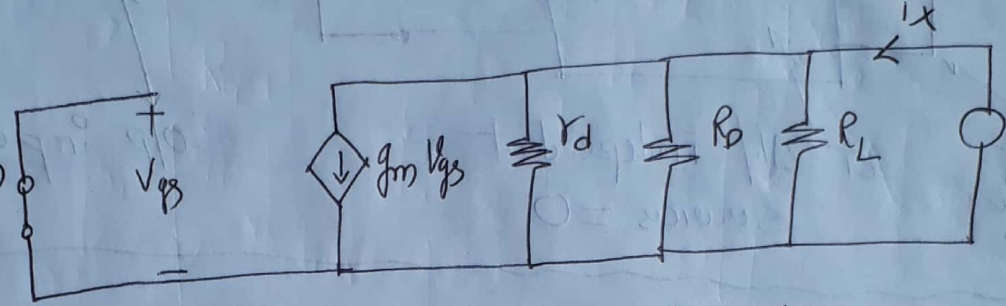
$$\boxed{R_{is} = R_{sig} + R_G}$$

Output impedance :-

Set $V_{in} = 0$

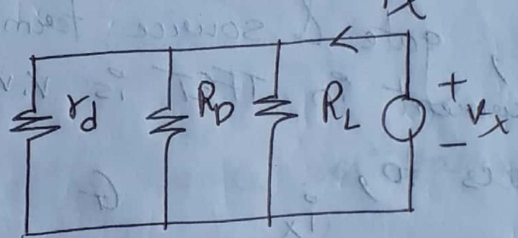


Refer ckt ©,



→ Since $V_{in} = 0$; and $V_{gs} = V_{in} = 0$

$g_m V_{gs} = 0$ → it becomes open ckt



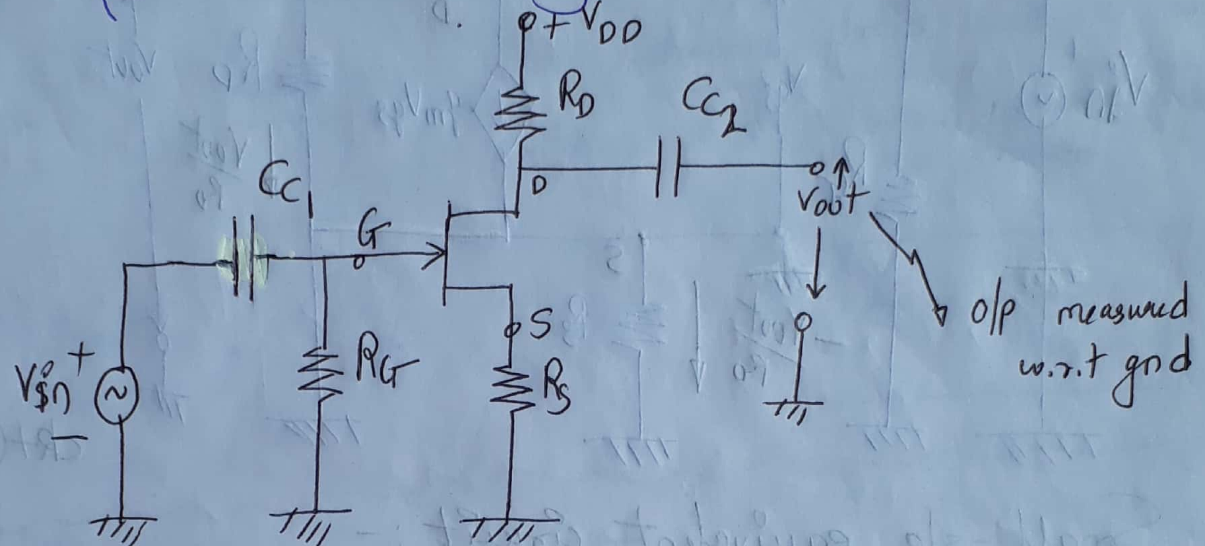
$$\frac{V_x}{i_x} = r_d \,||\, R_D \,||\, R_L$$

$$\boxed{R_o = r_d \,||\, R_D \,||\, R_L}$$

o/p impedance

2. Degenerated Common-Source amplifier :-

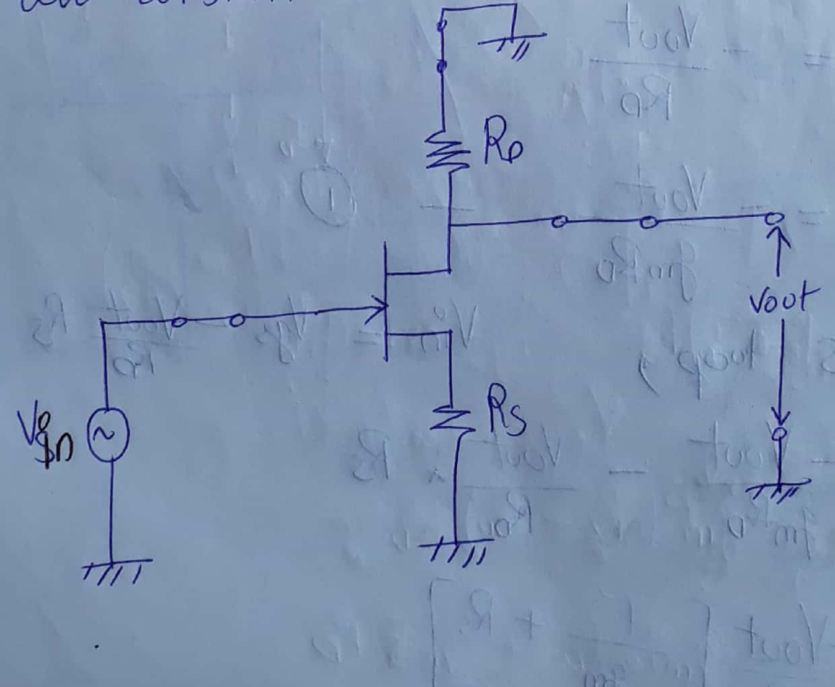
(Common-source stage with R_S unbypassed)



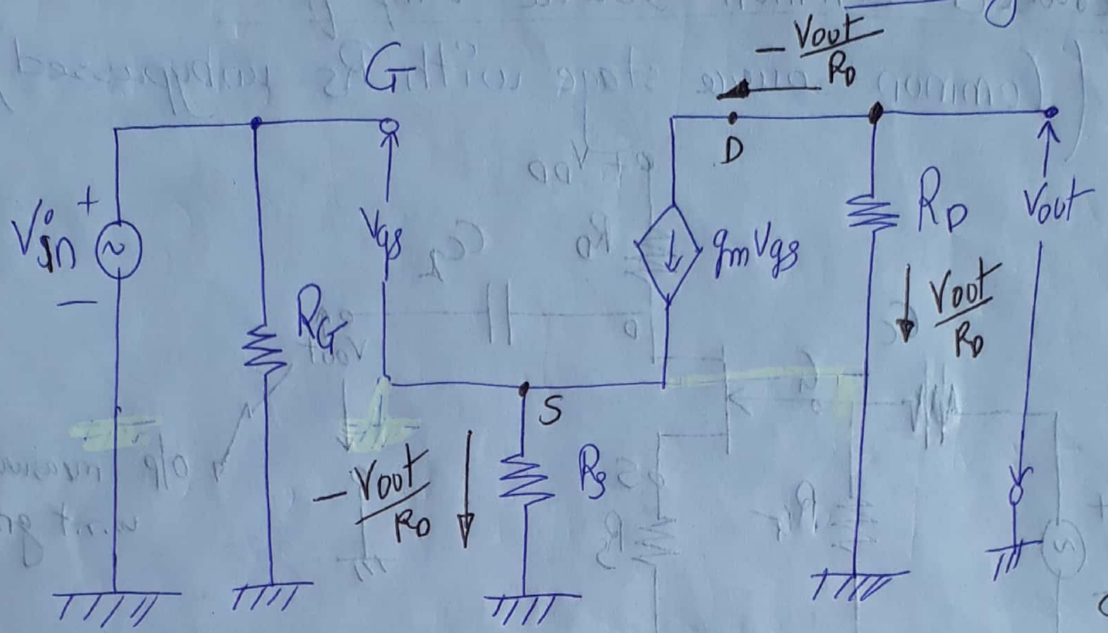
AC analysis :-

1) Set all capacitors as short-ckt (assuming mid-freq^n)

2) Set all constant dc sources as short-ckt



Assuming $r_d = \infty$



ckt (d)

Small-slg equivalent circuit :-

i] Voltage gain (A_v):

$$\boxed{A_v = \frac{V_{out}}{V_{in}}}$$

Observations:-

- $g_m V_{gs} = -\frac{V_{out}}{R_D}$

ie $V_{gs} = -\frac{V_{out}}{g_m R_D}$ — (1)

KVL in G-S loop, $V_{in} = V_{gs} - \frac{V_{out}}{R_D} R_S$

$$\rightarrow V_{in} = -\frac{V_{out}}{g_m R_D} - \frac{V_{out}}{R_D} \times R_S$$

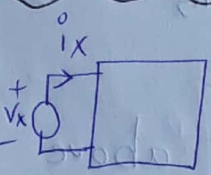
$$V_{in} = \frac{-V_{out}}{R_D}\left[\frac{1}{g_m} + R_S\right]$$

$$\boxed{A_v = \frac{V_{out}}{V_{in}} = \frac{-R_D}{\frac{1}{g_m} + R_S}}$$

$$A_v = -\frac{\text{Resistance tied between drain and ac ground}}{\frac{1}{g_m} + \text{Resistance tied between source and ac ground}}$$

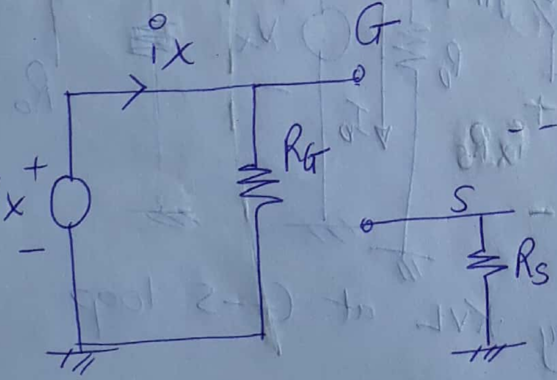
Simplification, If $\frac{1}{g_m} << R_S \Rightarrow \boxed{A_v \approx -\frac{R_D}{R_S}}$

Input impedance :-



Refer ckt d,

→ Due to open-circuit betn G & S, we have

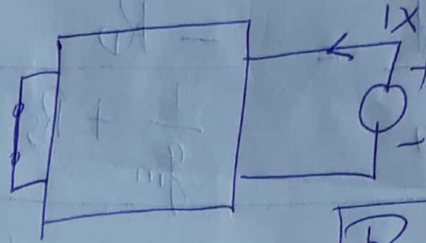


$$R_i = \frac{V_x}{i_x}$$

$$\boxed{R_i = R_G}$$

I/P impedance (Z_i)
OR I/P resistance (R_i)

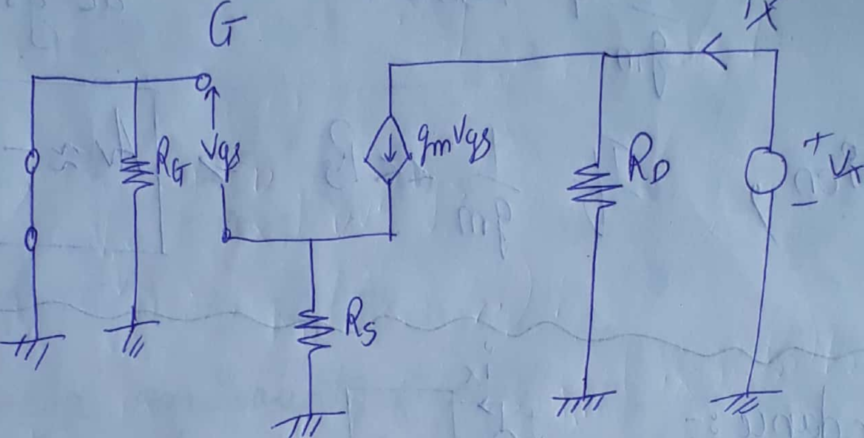
Output impedance :-



$$\boxed{R_o = \frac{V_x}{i_x}}$$

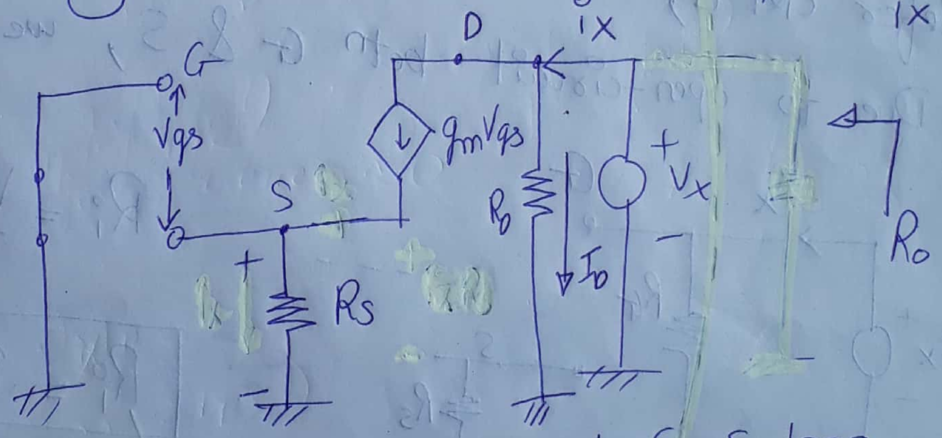
Refer ckt (d),

Set $V_{in} = 0$



Redrawing the above ckt as

$$R_o = \frac{V_x}{i_x}$$



KCL at 'D' node,

$i_x + g_m V_{gs} = I_o$

ie $i_x - I_o = g_m V_{gs}$

$\rightarrow V_{gs} = -(i_x - I_o) R_s$ -- by KVL at G-S loop

ie $i_x - I_o = -g_m (i_x - I_o) R_s$

$i_x - I_o = -g_m i_x R_s + g_m I_o R_s$

ie $i_x \cancel{(1+g_m R_s)} = + I_D \cancel{(1+g_m R_s)}$

ie $\boxed{i_x = I_D}$

This means $g_m V_{gs}$ source $\simeq 0$ for the applied conditions $\rightarrow$ as no current flows thr. $g_m V_{gs}$ it is considered as open-circuited

ie $V_x = i_x R_D$

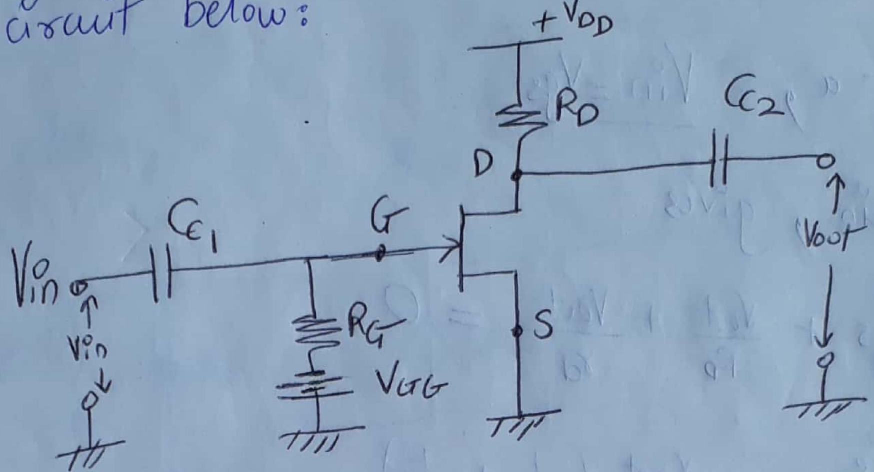
ie $\frac{V_x}{i_x} = R_D$

ie $\boxed{R_o = R_D}$

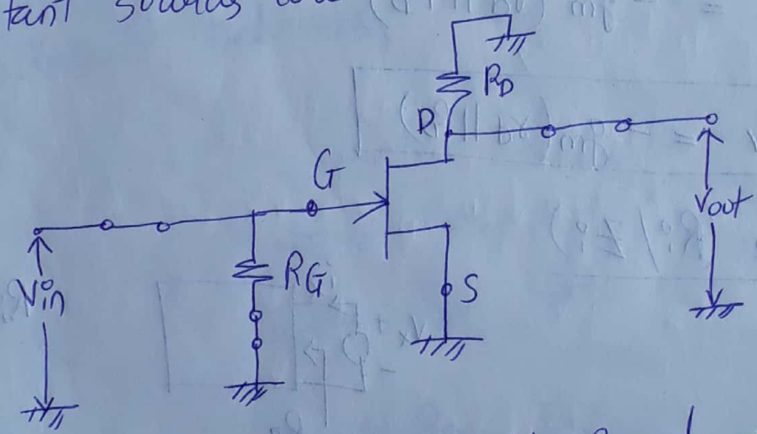
o/p impedance of the ckt

01
12/10/19

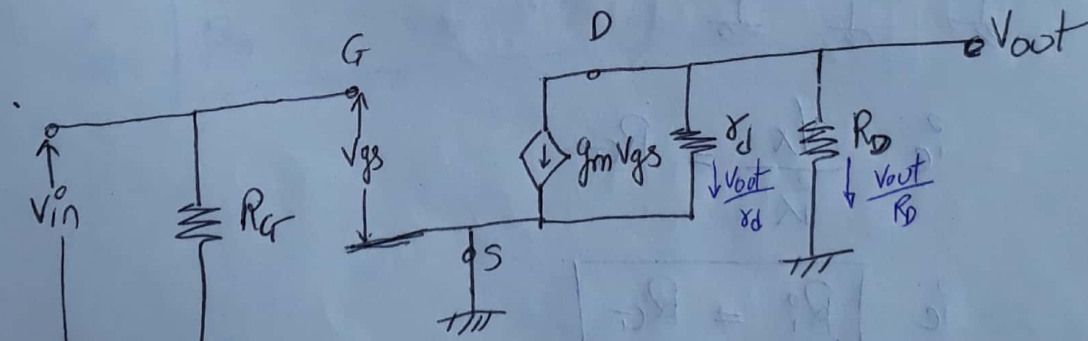
* Derive the expressions of A_v, R_i & R_o for the circuit below:



Sol^n: For small-signal AC analysis, all capacitors & constant sources are short-circuited



Now, replacing JFET with small-signal model



ckt(a): Small-signal equivalent circuit

1. Voltage gain (A_v) :

From ckt a, $V_{in} = V_{gs}$

KCL at 'Drain', gives

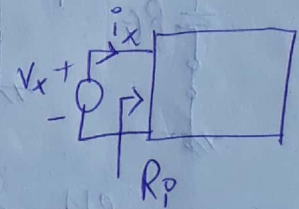
$$g_m V_{gs} + \frac{V_{out}}{R_D} + \frac{V_{out}}{r_d} = 0$$

$$g_m V_{in} = -V_{out}\left(\frac{1}{R_D} + \frac{1}{r_d}\right)$$

$$\frac{V_{out}}{V_{in}} = -g_m (r_d \| R_D)$$

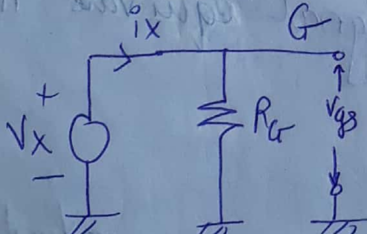
ie $\boxed{A_v = -g_m (r_d \| R_D)}$

2. I/P impedance (R_i / Z_i)



$R_i = \frac{V_x}{i_x}$

From ckt a,



Since gate current is zero, entire current i_x flows through R_G

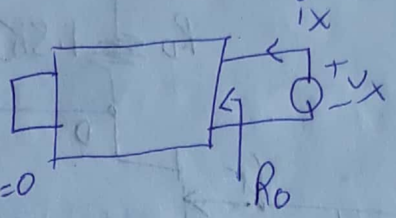
ie $\frac{V_x}{i_x} = R_G$

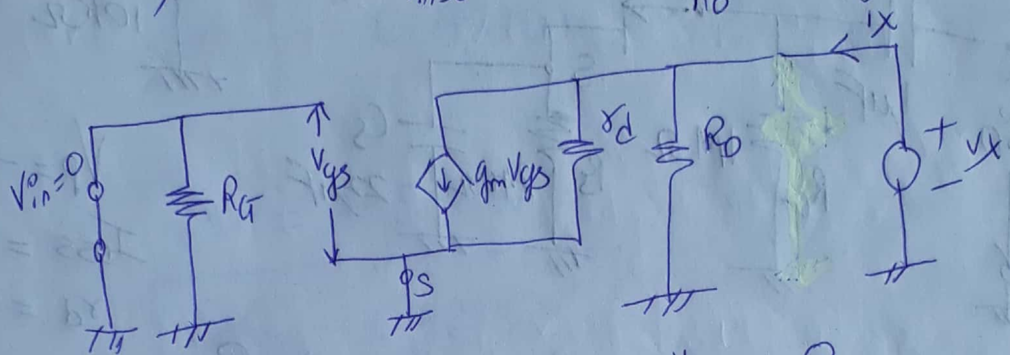
ie $\boxed{R_i = R_G}$

3. O/P impedance R_o / Z_o :

$$R_o = \frac{V_x}{i_x}$$

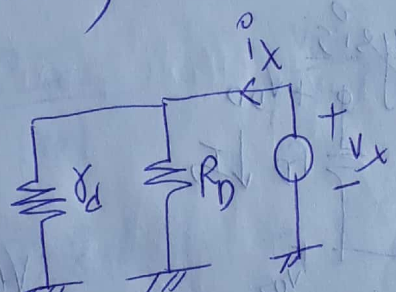
Refer ckt a,





Since $V_{in}=0$; $V_{gs}=0$; $g_m V_{gs} = 0$

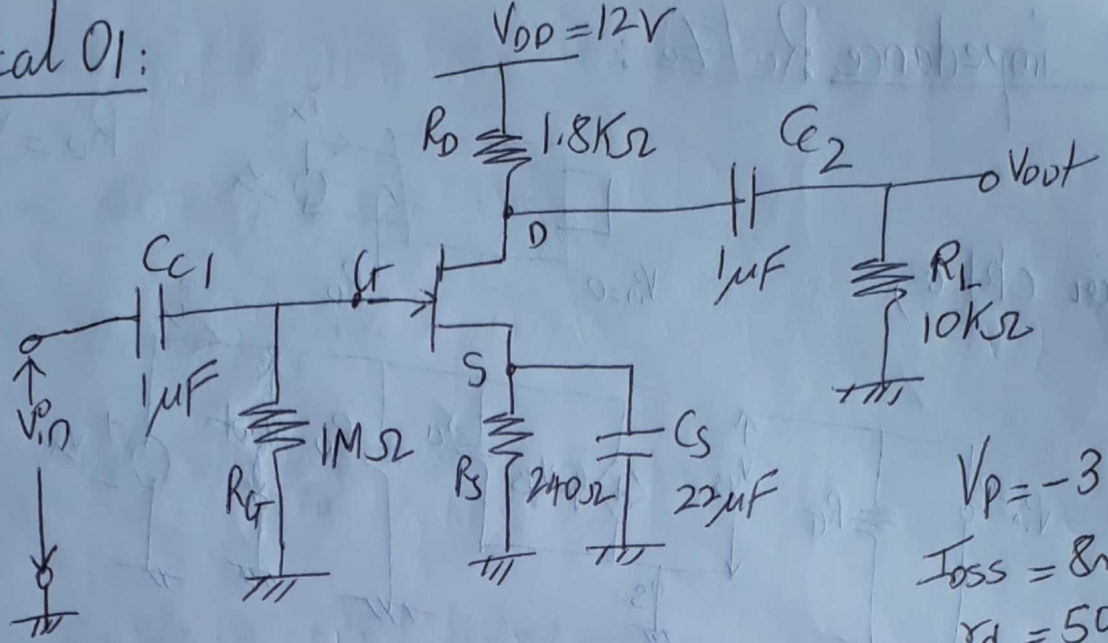
Circuit becomes,



i.e $\dfrac{V_x}{i_x} = r_d \| R_D$

i.e $\boxed{R_o = r_d \| R_D}$

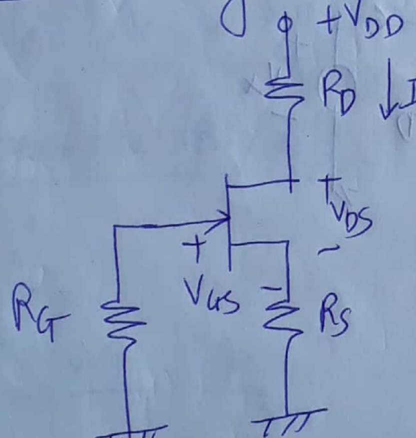
Numerical 01:



$V_P = -3V$
$I_{DSS} = 8mA$
$r_d = 50K\Omega$

Find 1) g_m 2) A_v 3) R_i & 4) R_o

Sol:- 1) DC Analysis



$V_G = 0$

$V_S = I_D R_S$

$V_{GS} = -I_D R_S$

$V_{GS} = -I_D(240)$ — ①

Assuming that JFET is working in saturation region,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 8mA\left(1 + \frac{V_{GS}}{3}\right)^2 \quad — ②$$

Put ② in ①, we get

$$V_{GS} = -1.92\left(1 + \frac{2}{3}V_{GS} + \frac{V_{GS}^2}{9}\right)$$

$$V_{GS} = -1.92 - 1.28V_{GS} - 0.2133V_{GS}^2$$

ie $0.2133V_{GS}^2 + 2.28V_{GS} + 1.92 = 0$

$$V_{GS} = -0.9215V \checkmark$$ (We select this as $V_{GS} > V_P$)

OR

$$V_{GS} = -9.76V$$

$$\therefore \boxed{V_{GS} = -0.9215V}$$

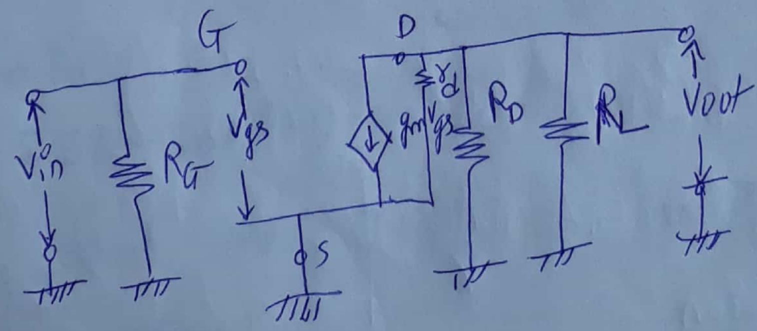
2) Find small-signal parameters g_m:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= \frac{2 \times 8mA}{3}\left(1 - \frac{(-0.9215)}{(-3)}\right)$$

$$\boxed{g_m = 3.693\frac{mA}{V}}$$

3) Small-signal AC analysis:



$\rightarrow A_v = -g_m (r_d \| R_D \| R_L)$

$= -g_m (1.48 K\Omega)$

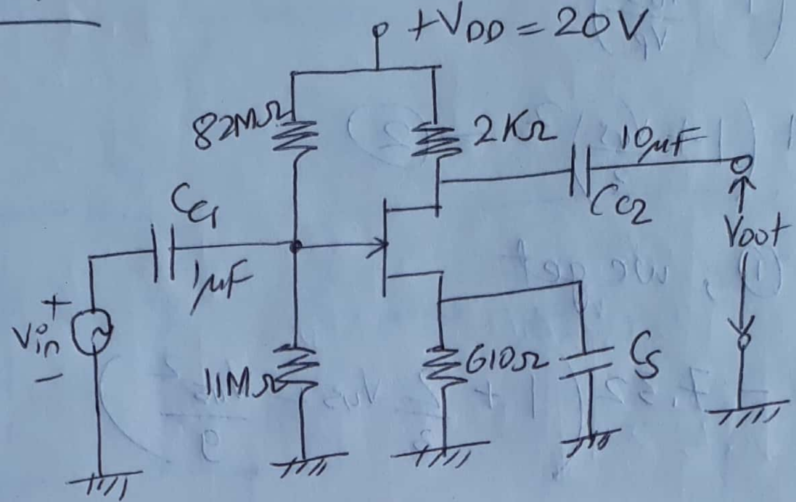
$\boxed{A_v = -5.46}$

$\rightarrow \boxed{R_i = R_G = 1M\Omega}$

$\rightarrow R_o = r_d \| R_D \| R_L$

$\boxed{R_o = 1.48 K\Omega}$

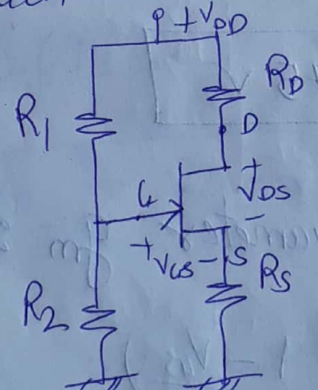
Numerical 02 :



$I_{DSS} = 12mA$
$V_P = -3V$

Find 1) g_m
2) A_v, R_i & R_o with R_S bypassed
3) A_v with R_S unbypassed

Sol^n :- 1) DC Analysis
All capacitors behaves as open-ckt



$V_G = \frac{R_2}{R_1+R_2} \times V_{DD}$

$= \frac{11M\Omega \times 20}{(11M + 82M)}$

$V_G = 2.36V$

. $V_S = I_D R_S$
. $V_{GS} = 2.36 - I_D(610)$ — (1)

Assuming that the JFET is working in saturation region

$$\rightarrow I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 12mA\left(1 + \frac{V_{GS}}{3}\right)^2 \quad \text{--- (2)}$$

Put (2) in (1), we get

$$V_{GS} = 2.36 - 7.32\left(1 + \frac{2}{3}V_{GS} + \frac{V_{GS}^2}{9}\right)$$

$$V_{GS} = 2.36 - 7.32 - 4.88\,V_{GS} - 0.8133\,V_{GS}^2$$

ie $0.8133\,V_{GS}^2 + 5.88\,V_{GS} + 4.96 = 0$

$V_{GS} = -0.975V$ ✓ (Since $V_{GS} > V_P$, use this value)

OR

$V_{GS} = -6.25V$

$\therefore \boxed{V_{GS} = -0.975\,V}$

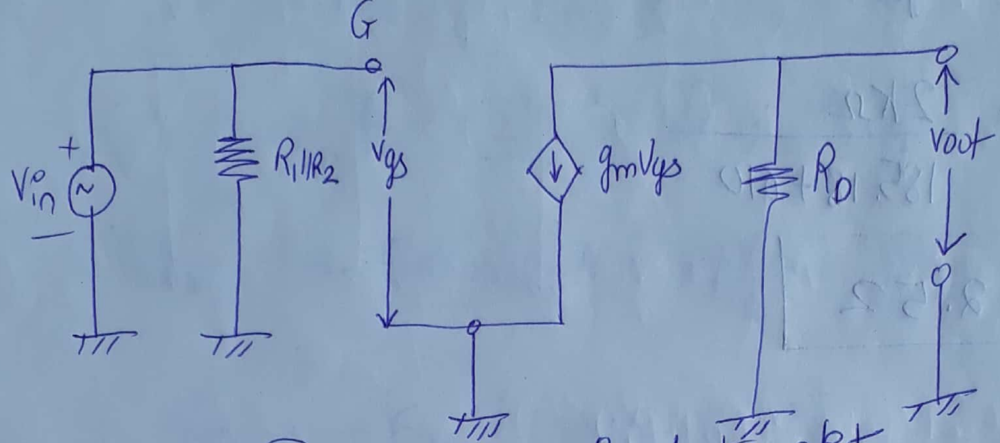
2) → Small-signal parameter g_m :

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= \frac{2\times 12mA}{3}\left(1 - \frac{(-0.975)}{(-3)}\right)$$

$$\boxed{g_m = 5.4\,\frac{mA}{V}}$$

Case ①: R_s is bypassed (rd not given, so assume $r_d = \infty$)



Small-s/g equivalent ckt

→ $A_v = -g_m R_D = -5.4 \frac{mA}{V} \times 2K\Omega$

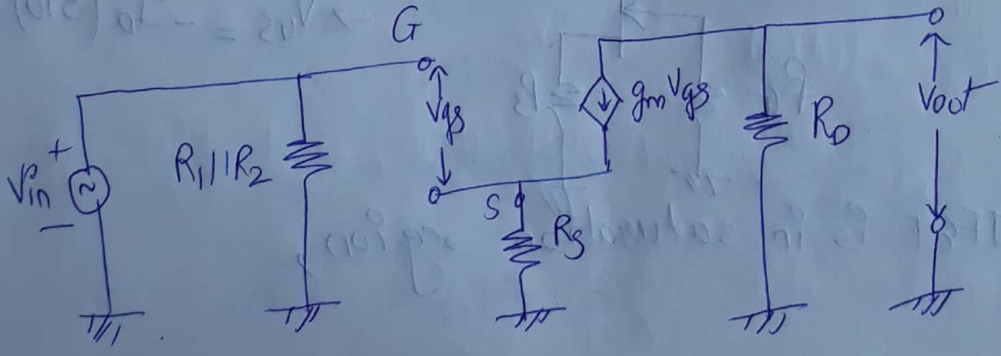
$\boxed{A_v = -10.8}$

→ $R_i = R_1 || R_2 = 82M || (11M\Omega)$

$\boxed{R_i = 9.69 M\Omega}$

→ $\boxed{R_o = R_D = 2K\Omega}$

Case ②: R_s is unbypassed

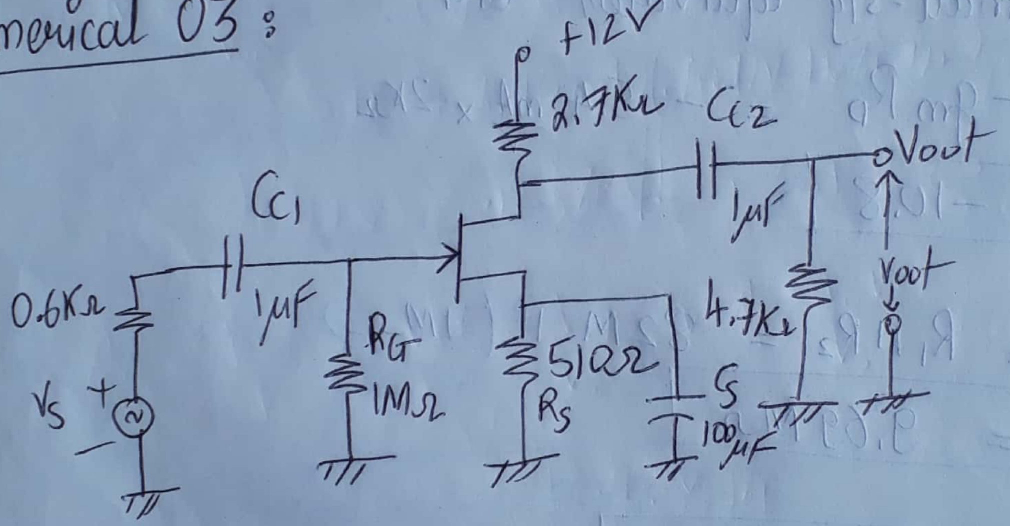


$$A_V = -\frac{R_D}{\frac{1}{g_m} + R_S}$$

$$= -\frac{2K\Omega}{185.18 + 610}$$

$$\boxed{A_V = -2.52}$$

Numerical 03 :

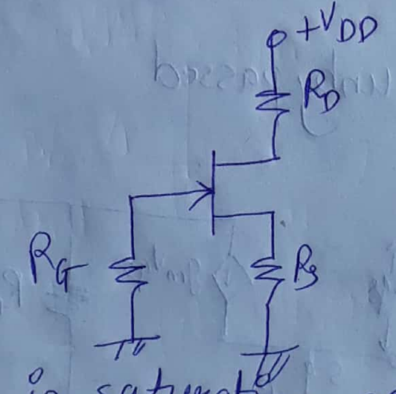


$I_{DSS} = 10mA$

$V_P = -6V$

Find A_V, R_i & R_o

Soln:- i) DC Analysis



$V_G = 0$

$V_S = I_D R_S$

$\rightarrow V_{GS} = -I_D(510)$ — (1)

Assuming JFET is in saturation region,

$$\rightarrow I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 10mA\left(1 + \frac{V_{GS}}{6}\right)^2 \quad - ②$$

$I_D \Rightarrow$ Put ② in ①, we get

$$V_{GS} = -510 \times 10mA\left(1 + \frac{2V_{GS}}{6} + \frac{V_{GS}^2}{36}\right)$$

$$V_{GS} = -5.1\left(1 + \frac{V_{GS}}{3} + \frac{V_{GS}^2}{36}\right)$$

$$V_{GS} = -5.1 - 1.7V_{GS} - 0.1417V_{GS}^2$$

$$\rightarrow 0.1417V_{GS}^2 + 2.7V_{GS} + 5.1 = 0$$

ie $V_{GS} = -2.12\,V$ ✓ (We select this value since $V_{GS} > V_P$)

OR

$V_{GS} = -16.92\,V$

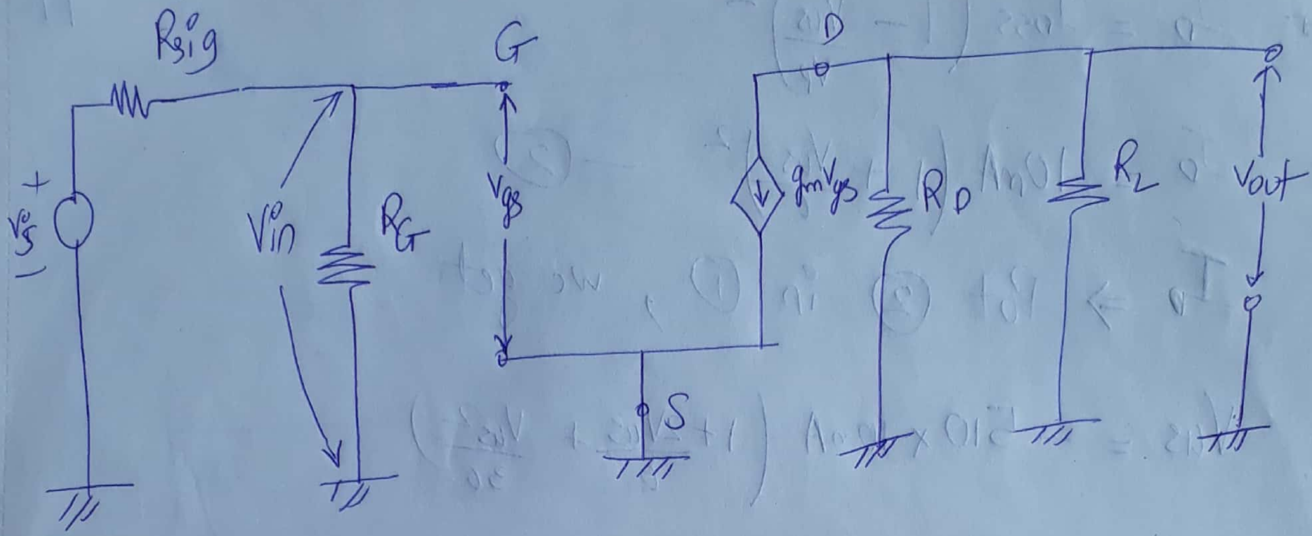
$$\therefore \boxed{V_{GS} = -2.12V}$$

2) Small-signal parameter gm:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= \frac{2 \times 10mA}{6}\left(1 - \frac{(-2.12)}{(-6)}\right)$$

$$\boxed{g_m = 2.15\ \frac{mA}{V}}$$



$\rightarrow$ $A_v = \frac{V_{out}}{V_{in}} = -g_m (R_D \| R_L)$

$= -2.15\,mA\,(2.7K \| 4.7K)$

$\boxed{A_v = -3.687}$

$\rightarrow$ $A_{vs} = \frac{V_{out}}{V_s} = \frac{V_{out}}{V_{in}} \times \frac{V_{in}}{V_s} = A_v \frac{V_{in}}{V_s}$

$\frac{V_{in}}{V_s} = \frac{R_G}{R_G + R_{sig}} = 0.9994$

ie $A_{vs} = A_v \times 0.9994 = -3.687 \times 0.9994$

$\boxed{A_{vs} = -3.684}$

$\rightarrow$ $R_i = R_G = 1M\Omega$

$\rightarrow$ $R_O = R_D \| R_L = 2.7K \| 4.7K\Omega = \underline{1.714\,K\Omega}$