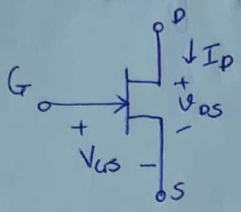
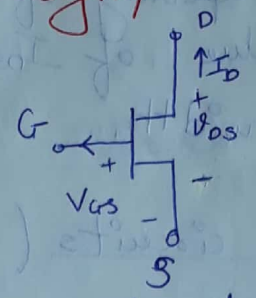
JFET DC Biasing: (Design)

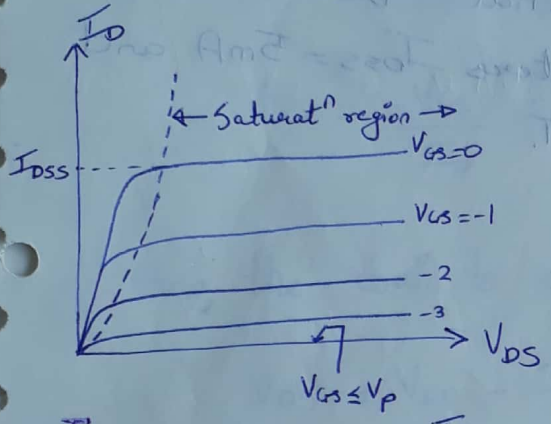
M.2.1 01/02/2015

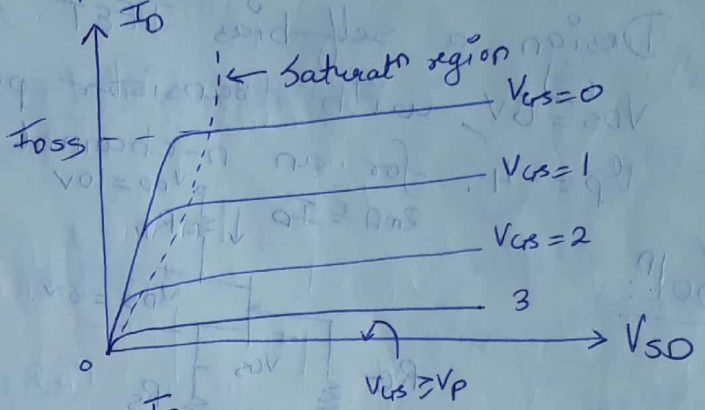


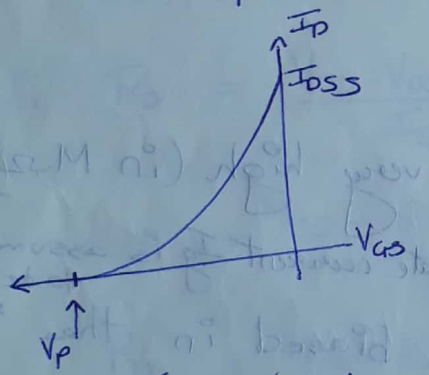
n-channel JFET



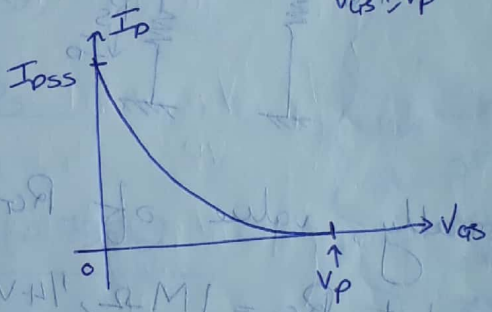
p-channel JFET







V_p is -ve for n-channel JFET



V_p is +ve for p-channel JFET

INDERJIT SINGH

- The ideal I-V characteristics, when the transistor is biased in the saturation region are,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

where, I_{DSS} is saturation current when $V_{GS}=0$, V_p → Pinch-off voltage.

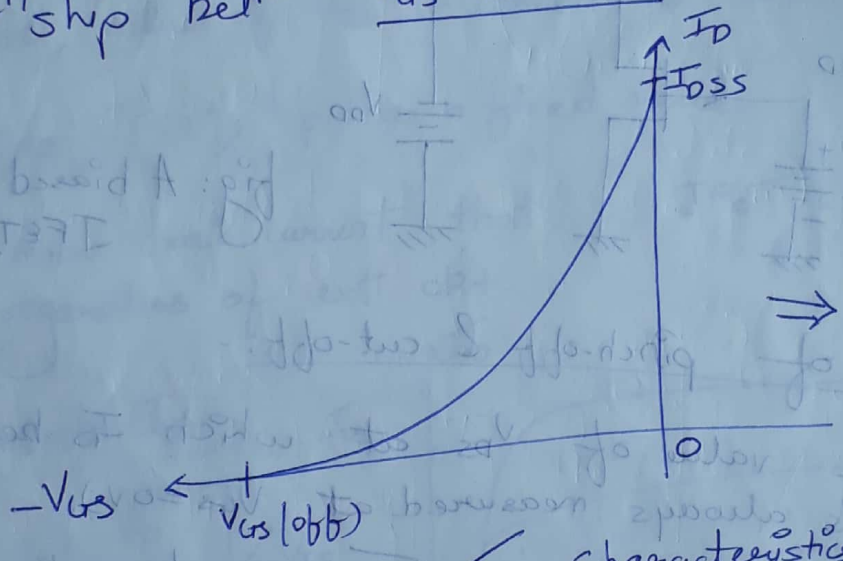
- For n-channel JFET, saturation region occurs when $V_{DS} \geq V_{DS(sat)}$ where, $V_{DS(sat)} = V_{GS} - V_p$
- For pchannel JFET, saturation region occurs when $V_{SD} \geq V_{SD(sat)}$ where, $V_{SD(sat)} = V_p - V_{GS}$.

* JFET Transfer characteristic:

→ We have seen that a range of V_{GS} values from zero to $V_{GS(off)}$ controls the amount of drain current

• For an n-channel JFET, $V_{GS(off)}$ is -ve. & for a p-channel JFET, $V_{GS(off)}$ is +ve.

Relat^{n}ship ♡ betn V_{GS} and I_D:



⇒ "Non-Linear Curve"

fig b) JFET (n-channel) transfer characteristics curve.

• This curve, shows the operating limits of a JFET,

ie $I_D = 0$ when $V_{GS} = V_{GS(off)}$.

and $I_D = I_{DSS}$ when $V_{GS} = 0$.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

OR V_P

→ Thus I_D can be found if $V_{GS(off)}$ and I_{DSS} are known.

* JFET → a square-law device!

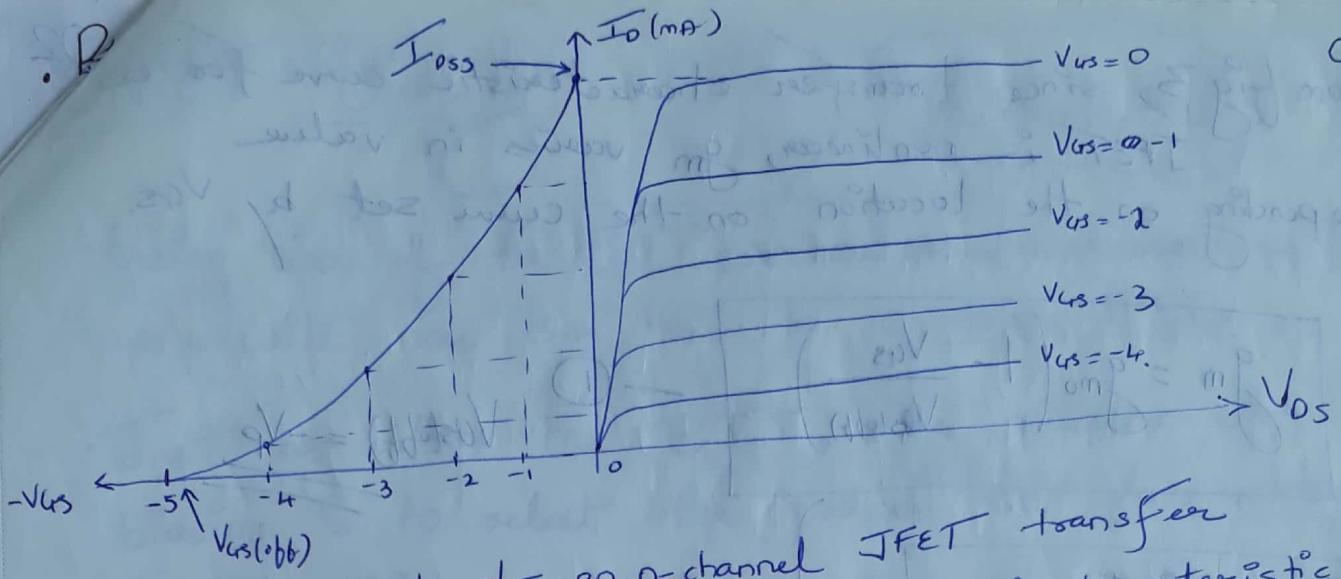


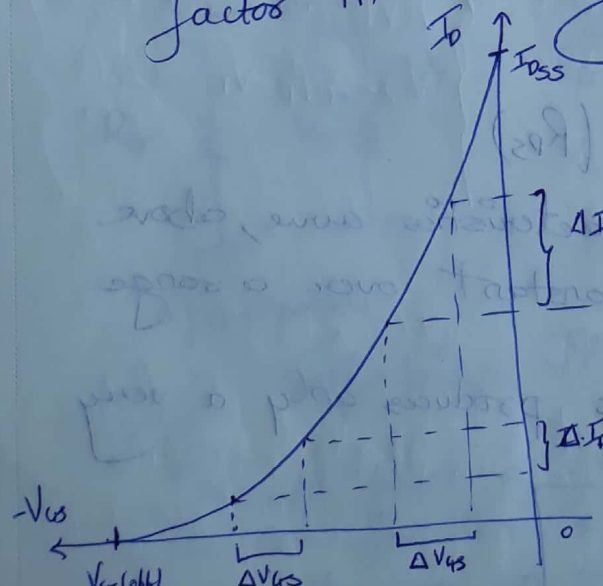
fig: Development of an n-channel JFET transfer characteristics curve from JFET drain characteristic curve.

* JFET Forward transconductance: (g_m)

↳ It is the change in drain current (ΔI_D) for a given in gate to source voltage (ΔV_{GS}) For a V_{DS} constant.

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}=\text{constant}}$$

* g_m is important in FET amplifiers as a major factor in determining the voltage gain.



$g_{m_2} = \frac{\Delta I_{D_2}}{\Delta V_{GS}}$

$g_{m_2} > g_{m_1}$

$g_{m_1} = \frac{\Delta I_{D_1}}{\Delta V_{GS}}$

fig 3: g_m variation depending on the bias point (V_{GS})

INDERJIT SINGH

4/10/19

Biasing circuits for JFET

1. Fixed bias
2. Self bias
3. Voltage-divider bias

Fixed Bias circuit:-

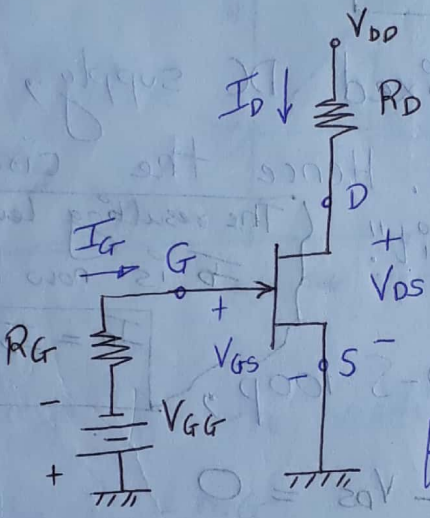


fig 1.1

JFET is n-channel

- The simplest biasing arrangement for n-channel JFET is fixed bias configuration.
- for the dc analysis,

$$I_G \cong 0$$

$$\therefore V_{R_G} = I_G R_G \approx 0V$$

{ The zero-volt drop across R_G permits replacing R_G by a short-circuit equivalent. }

DC Analysis:

Gate-source voltage V_{GS}:

→ Applying KVL to the input loop ie G-S loop

$$-V_{GG} - I_G R_G - V_{GS} = 0$$

For JFET, $I_G = 0$

ie $\boxed{V_{GS_Q} = -V_{GG}}$

Since V_{GG} is a fixed DC supply, the voltage V_{GS} is fixed in magnitude. Hence the circuit is called as "fixed-bias circuit".

The resulting level of drain current I_D is now controlled by equation

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

→ Applying KVL to D-S loop,

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$\boxed{V_{DS_Q} = V_{DD} - I_D R_D}$$

→ $\boxed{V_S = 0}$

→ $\boxed{V_D = V_{DD} - I_D R_D}$

OR

$V_{DS} = V_D - V_S \rightarrow V_D = V_{DS} + V_S = V_{DS}$

ie $\boxed{V_D = V_{DS}}$

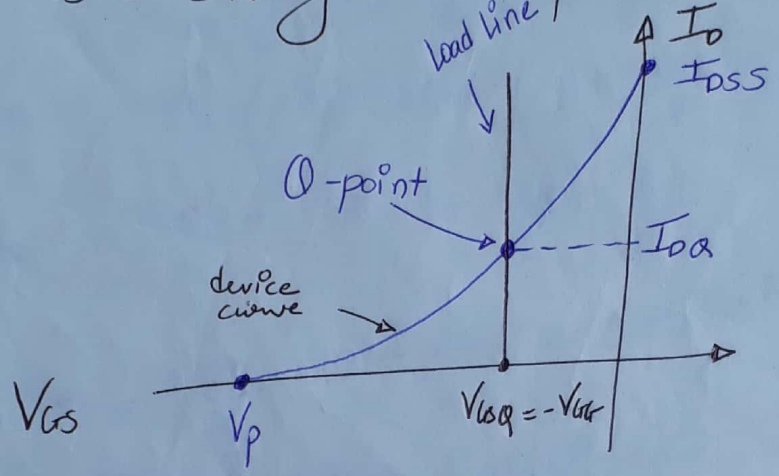
→ $\boxed{V_G = V_{GS}}$

• DC Load Line :-

Equation of load Line

$$V_{GS_Q} = -V_{GG}$$

→ It is a straight Line parallel to y-axis



→ At any point on the vertical line (load Line), the level of V_{GS} is $-V_{GG}$.

→ The point where the two curves intersect is the common solution to the configuration — commonly referred to as the "Q-point" or "operating point".

• Limitation: Since this circuit requires two dc supplies its use is Limited & it is not commonly used.

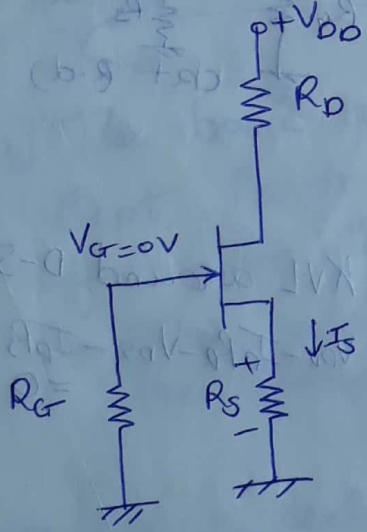
JFET Biasing:

g_m, $V_{GS(off)}$, I_{DSS}

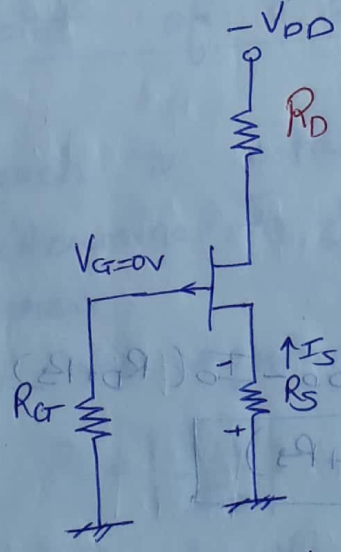
- Using some of the FET parameters discussed so far, we will now see how to dc-bias JFETs.
- Just as with the BJT, the purpose of biasing is to select the proper dc V_{GS} voltage to establish a desired value of drain current I_D, and thus; a proper Q-point (I_D, V_{GS}).

Two types of biasing ckts:-

1] Self-bias:-



a) n-channel



b) p-channel

Fig 2 self-bias JFET's ($I_S = I_D$ in all FETs)

- Recall that a JFET must be operated such that the G-S junction is always R.B. This condition requires a -ve V_{GS} for an n-channel JFET and a +ve V_{GS} for an p-channel JFET.

INDERJIT SINGH

• This can be achieved using the self-bias arrangement as shown in fig 2.

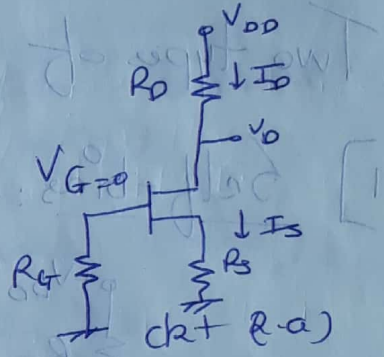
→ The gate resistor, R_G does not affect the bias because it has essentially no voltage drop across it. ∴ $V_G = 0V$.

• R_G is necessary only to isolate an ac sig from ground in amplifier applications.

For ckt 2.a),

• I_S produces a drop across R_S, & makes source +ve w.r.t ground.

∴ $I_S = I_D$ & $V_G = 0$, $V_S = I_D R_S$.



→ $V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$

$$\boxed{V_{GS} = -I_D R_S}$$

$V_D = V_{DD} - I_D R_D$

∴ $V_S = I_D R_S$ ⇒

$V_{DS} = V_D - V_S = V_{DD} - I_D(R_D + R_S)$

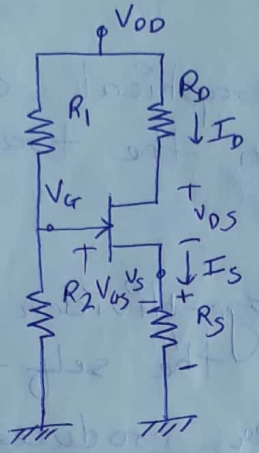
$$\boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)}$$

{ KVL around D-S
$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$ }

• Also, $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

Voltage-divider bias:-

An n-channel JFET with voltage-divider bias is shown below,



- The voltage at the source of the JFET must be more +ve than the voltage at the gate in order to keep the gate-source junction reverse-biased.

$$V_S = I_D R_S$$

- The gate voltage is set by resistors R_1 and R_2 whose expression by using voltage-divider formula is,

$$V_G = \left(\frac{R_2}{R_1+R_2}\right) V_{DD}$$

$$\boxed{V_{GS} = V_G - \left(\frac{R_2}{R_1+R_2}\right) V_{DD}}$$

- The gate to source voltage is

$$V_{GS} = V_G - V_S$$

$$\rightarrow V_S = V_G - V_{GS}$$

$$\cdot\ I_D = \frac{V_S}{R_S}$$

$$\text{ie } \boxed{I_D = \frac{V_G - V_{GS}}{R_S}}$$

KVL around D-S loop,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\text{ie } \boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)}$$

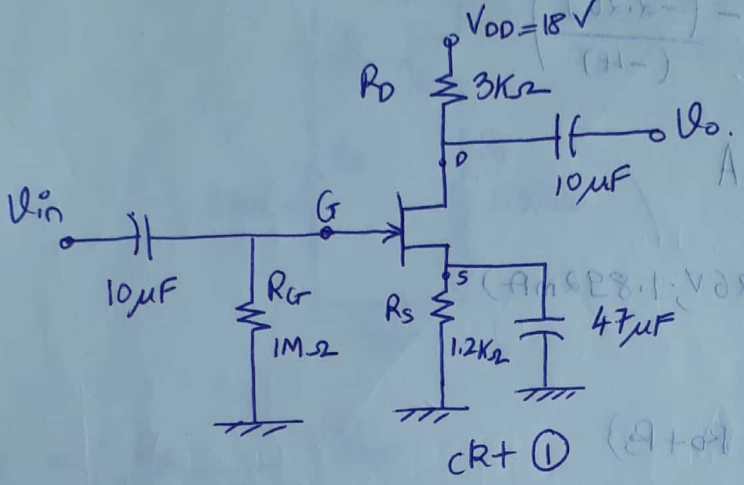
Also, $\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$

JFET Biasing (Numericals)

M2.1

Analytical method:

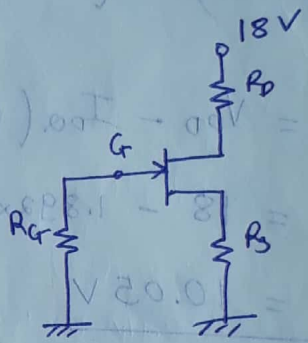
1] Determine the Q-point and V_{DS} for the ckt ①.



ckt ①

$I_{DSS} = 10mA$

$V_P = -4V$



- $V_G = 0$
- $V_S = I_D R_S = 1.2K(I_D)$
- $V_{GS} = V_G - V_S = -1.2K(I_D) \quad -①$
- $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

ie $I_D = 10\times10^{-3}\left(1 + \frac{V_{GS}}{4}\right)^2 \quad -②$

ie $V_{GS} = -1.2K \times 10\times10^{-3}\left(1 + \frac{V_{GS}}{4}\right)^2$

$V_{GS} = -12\left(1 + 0.25V_{GS}\right)^2$

$V_{GS} = -12\left(1 + 0.5V_{GS} + 0.0625V_{GS}^2\right)$

$V_{GS} = -12 - 6V_{GS} - 0.75V_{GS}^2$

$0.75V_{GS}^2 + 7V_{GS} + 12 = 0$

$V_{GS} = -2.26V$ ✓ and $V_{GS} = -7.07V$ ✗ (V_{GS} should be more than V_P)

INDERJIT SINGH

$V_{GS} = -2.26\,V$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 10\times10^{-3}\left(1 - \frac{(-2.26)}{(-4)}\right)^2$$

$$I_{DQ} = 1.892\ mA$$

$$Opt \equiv (V_{GSQ}, I_{DQ}) \equiv (-2.26\,V, 1.892\,mA)$$

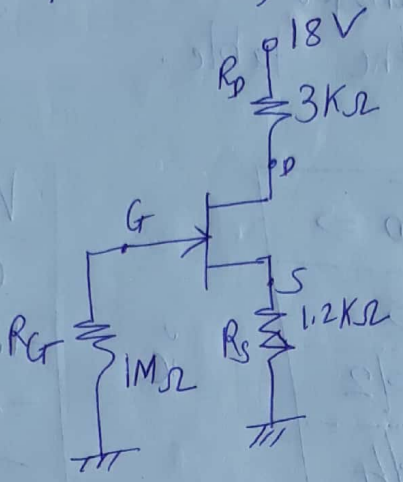
$$\cdot\ V_{DSQ} = V_{DD} - I_{DQ}(R_D + R_S)$$

$$= 18 - 1.892\times10^{-3}(3K + 1.2K)$$

$$V_{DSQ} = 10.05\,V$$

• Determine I_{DQ} & V_{GSQ}, V_{DS} for the ckt below

Graphically



$I_{DSS} = 10mA$

$V_P = -4V$

Soln: We will adopt graphical approach,

From ckt, $V_G = 0$ --- (as $I_G = 0$)

$V_S = I_D R_S$

ie $\boxed{V_{GS} = -I_D R_S}$ — ①

↳ Eqn of DC load line

1) Put $I_D = 0$, $V_{GS} = 0$ → 1st pt ≡ (0, 0)

2) Put $I_D = \frac{I_{DSS}}{2}$ ⇒ $V_{GS} = -\frac{I_{DSS}}{2} \times R_S = \frac{-10mA \times 1.2K\Omega}{2}$

$I_D = \frac{10mA}{4}$

$I_D = 2.5mA$

$V_{GS} = -3V$

→ 2nd pt ≡ (−3, 2.5mA)

Plot load line using these two point co-ordinates

Next, we plot transfer curve in graph paper using the table.

$V_{GS} \Rightarrow$	$I_D \Rightarrow$
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0

$I_{DSS} = 10mA$
$V_P = -4V$

ie

V_{GS}	I_D
0	10mA
-1.2V	5mA
-2V	2.5mA
-4V	0

Plot transfer curve using this data

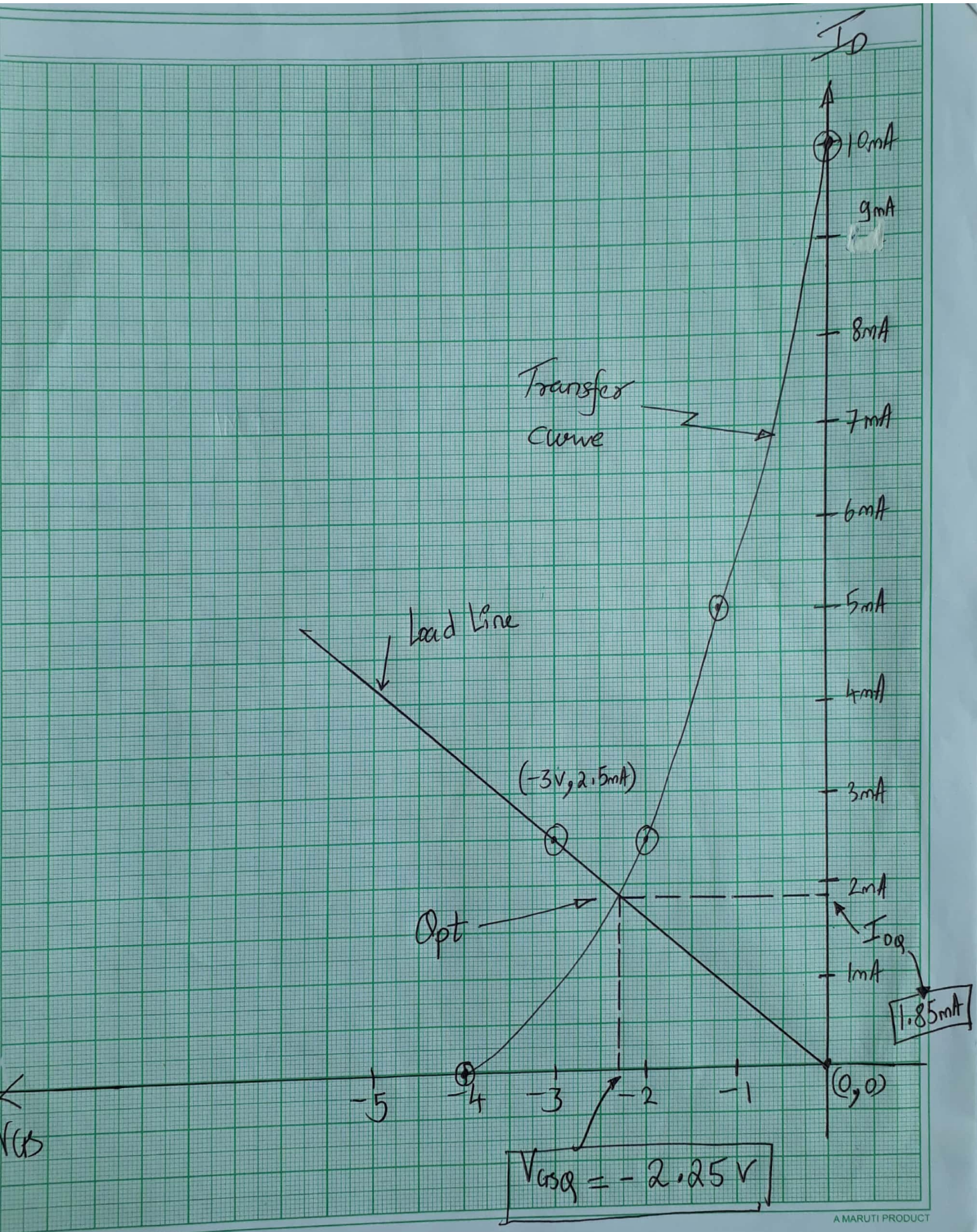
→ The intersection of load line & transfer curve gives the Q-point.

ie $V_{GSQ} = -2.25V$
$I_{DQ} = 1.85mA$ ⟶ Obtained graphically

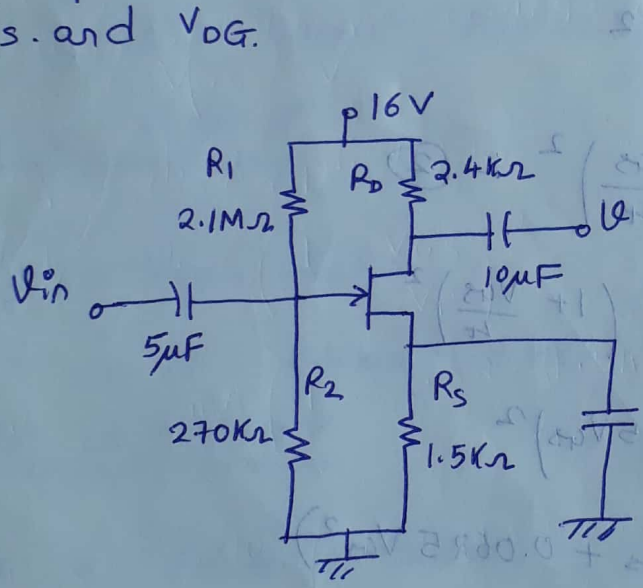
→ $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 18 - 1.85mA(3K + 1.2K)$

$V_{DS} = 10.23V$



2. Find Qpt and V_{DS} for ckt ②
V_D, V_S and V_{DG}.

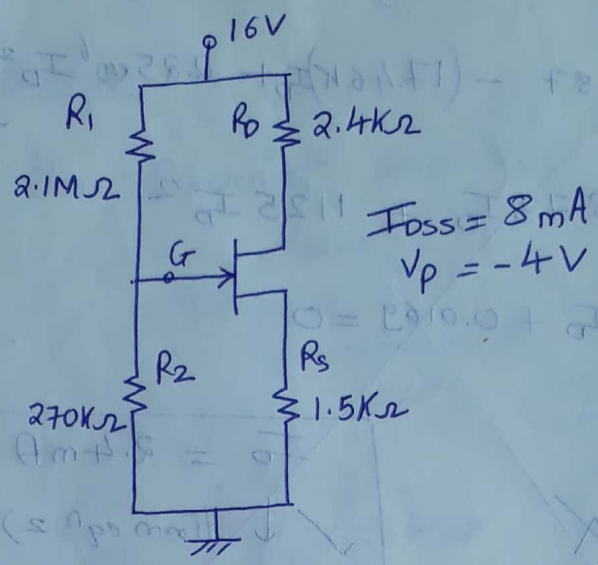


$I_{DSS} = 8mA$
$V_P = -4V$.

ckt ②

Solution: For DC Analysis, open circuit all the capacitors in the ckt.

DC equivalent of ckt ② is,



- $V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$

$V_G = \left(\frac{270K}{2.1M + 270K}\right) 16 = 1.82\ V$

- $V_S = I_D R_S = (1.5K) I_D$

- $V_{GS} = V_G - V_S$

$V_{GS} = 1.82 - (1.5K) I_D$

16/10/19

$V_{GS} = 1.82 - (1.5K)I_D$ — (1)

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

ie $I_D = 8mA\left(1 + \frac{V_{GS}}{4}\right)^2$ — (2)

Put (2) in (1), we get

$V_{GS} = 1.82 - (1.5K) \times 8mA\left(1 + \frac{V_{GS}}{2} + \frac{V_{GS}^2}{16}\right)$

$V_{GS} = 1.82 - 12\left(1 + \frac{V_{GS}}{2} + \frac{V_{GS}^2}{16}\right)$

ie $V_{GS} = 1.82 - 12 - 6V_{GS} - 0.75V_{GS}^2$

ie $0.75V_{GS}^2 + 7V_{GS} + 10.18 = 0$

ie $V_{GS} = -1.8V$ ✓ (we select this since $V_{GS} > V_P$)

OR

$-7.53V$ ✗

$\therefore$ $\boxed{V_{GS_Q} = -1.8V}$

Now, $I_D = 8mA\left[1 - \left(\frac{-1.8}{-4}\right)\right]^2$

$\boxed{I_{DQ} = 2.42mA}$

$Q_{pt} \equiv (-1.8V, 2.42mA)$

→ $V_{DS} = V_{DD} - I_{DQ}(R_D + R_S)$

$= 16 - 2.42mA\,(2.4K + 1.5K)$

$\boxed{V_{DS} = 6.56\,V}$

→ $V_D = V_{DD} - I_D R_D$

$= 16 - 2.42mA \times 2.4K$

$\boxed{V_D = 10.19}$

→ $V_S = I_{DQ} R_S$

$= 2.42mA \times 1.5K$

$\boxed{V_S = 3.63\,V}$

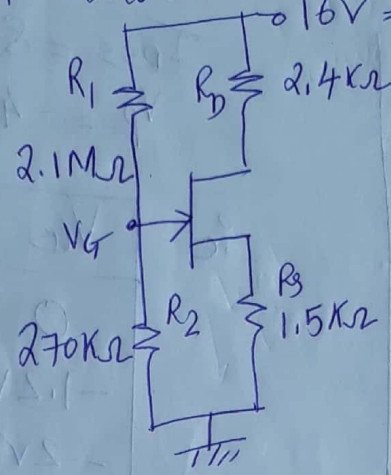
→ $V_{DG} = V_D - V_G$

$= 10.19 - 1.82$

$\boxed{V_{DG} = 8.37\,V}$

16/10/19

* Determine I_{DQ} and V_{GSQ} graphically for given ckt below:-



$I_{DSS} = 8mA$

$V_P = -4V$

Soln:- $V_G = \frac{R_2}{R_1+R_2} \times V_{DD} = \frac{270K}{270K+2.1M} \times 16$

$\boxed{V_G = 1.82V}$

$V_{GS} = V_G - V_S = 1.82 - I_D R_S = 1.82 - I_D(1.5K)$

ie $\boxed{V_{GS} = 1.82 + (1.5K) I_D}$ — (1)

↳ This is the eqn of load line

1) Put $I_D = 0$; $V_{GS} = 1.82$ → 1st pt: (1.82V, 0)

2) Put $V_{GS} = 0$ ⇒ $I_D = \frac{1.82}{1.5K} = 1.21mA$

2nd pt: (0, 1.21mA)

Plot load line with above two coordinates

To plot transfer curve on graph paper we use the following table

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0

$I_{DSS} = 8mA$

$V_P = -4V$

ie

V_{GS}	I_D
0	8mA
-1.2V	4mA
-2V	2mA
-4V	0

Plot transfer curve using this data

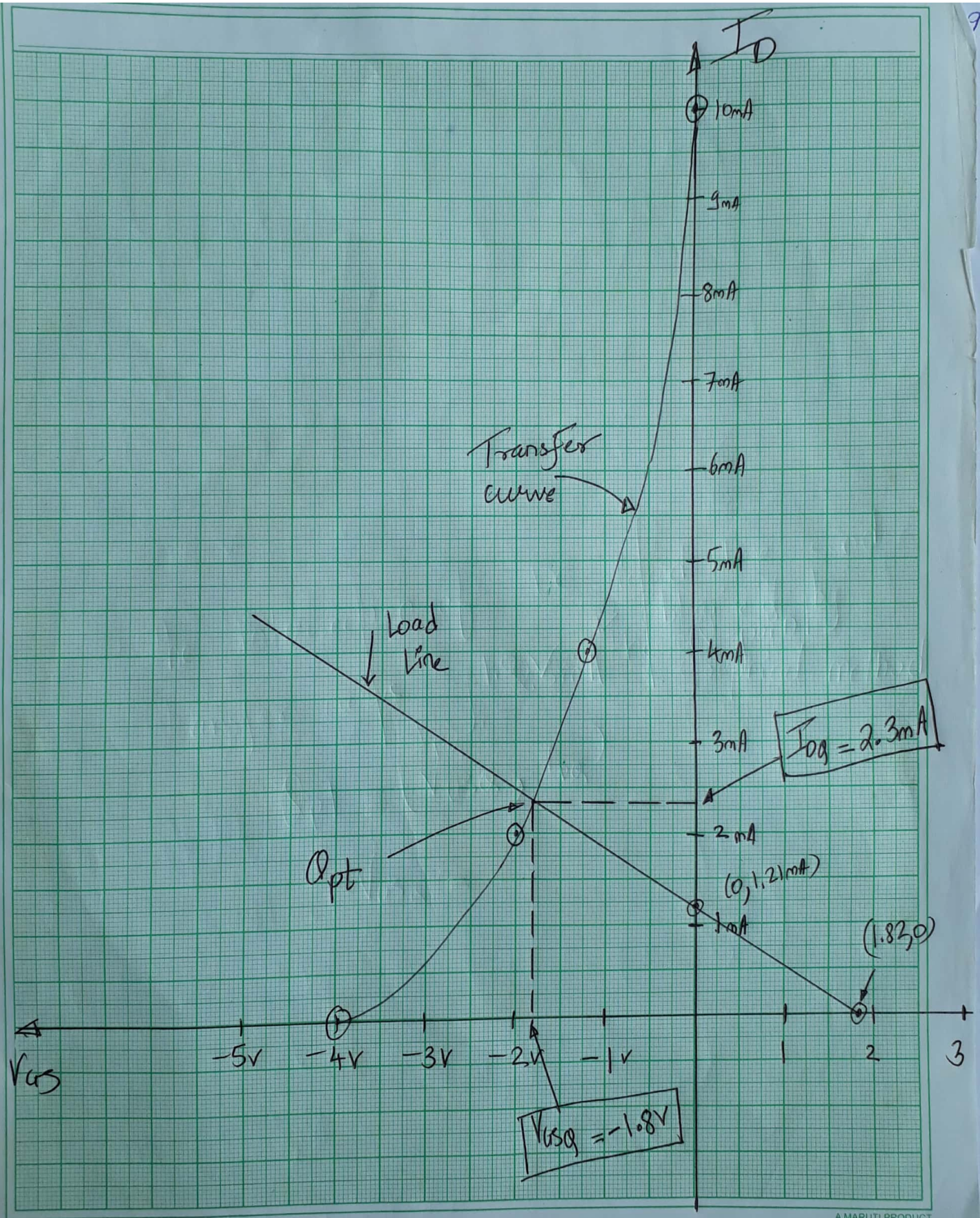
The intersection of DC load line and transfer curve gives us the Q-point

$Q_{pt} \equiv (V_{GSQ}, I_{DQ})$

$V_{GSQ} = -1.8V$

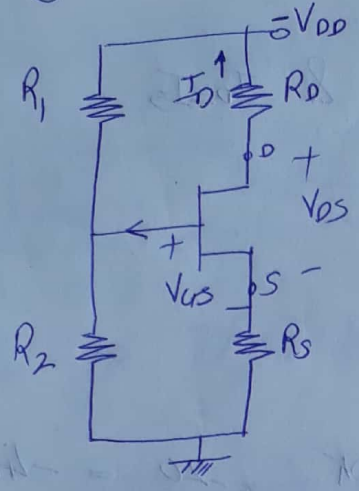
$I_{DQ} = 2.3mA$

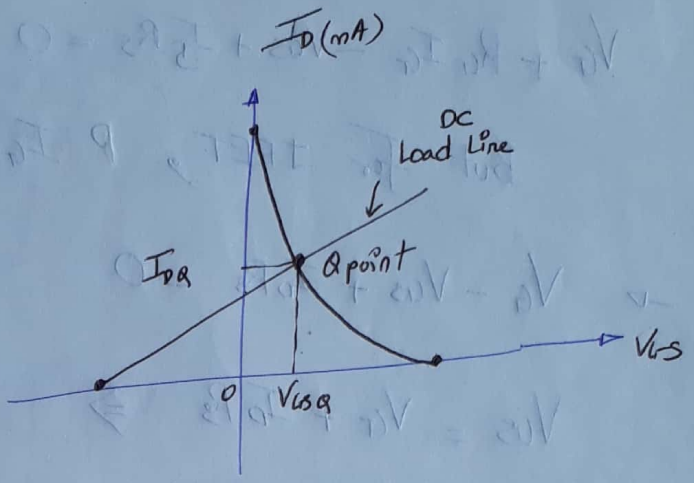
→ obtained by graphical method



7/10/19

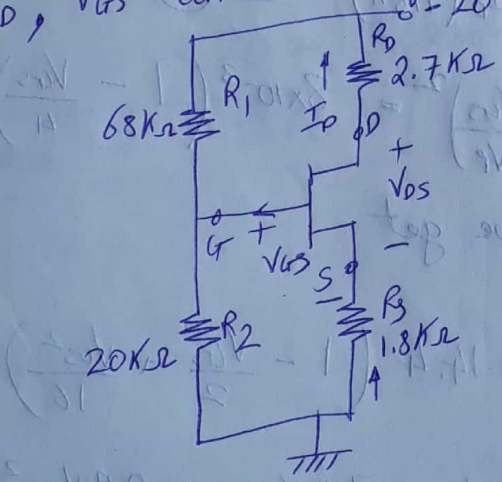
• Voltage-divider biasing (P-JFET) :-





Numerical 01:

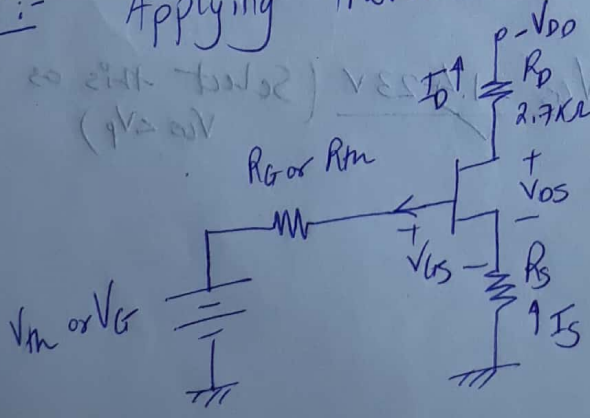
Find I_D, V_{GS} and V_{DS} for the circuit below:-



$I_{DS} = 8\,mA$

$V_P = 4V$

Soln:- Applying thevenin's at gate, we get



→ KVL to G-S loop,

$$V_G + R_G I_G - V_{GS} + I_S R_S = 0$$

But for JFET, $I_G = 0$ & $I_D = I_S$

→ $V_G - V_{GS} + I_D R_S = 0$

$$V_{GS} = V_G + I_D R_S \Rightarrow$$

→ $$V_{GS} = \frac{R_2}{R_1 + R_2}(-V_{DD}) = \frac{20K}{20K + 68K} \times -20 = -4.55V$$

ie $$V_{GS} = -4.55 + I_D(1.8K) \quad - (1)$$

→ $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8\times10^{-3}\left(1 - \frac{V_{GS}}{4}\right)^2 \quad - (2)$$

Put (2) in (1), we get

ie $$V_{GS} = -4.55 + 14.4\left(1 - \frac{V_{GS}}{2} + \frac{V_{GS}^2}{16}\right)$$

$$V_{GS} = -4.55 + 14.4 - 7.2V_{GS} + 0.9V_{GS}^2$$

ie $$0.9V_{GS}^2 - 8.2V_{GS} + 9.85 = 0$$

ie $V_{GS} = 7.68V$, $V_{GS} = 1.423V$ (Select this as $V_{GS} < V_P$)

→ $\boxed{V_{GSQ} = 1.423V}$

$$\rightarrow I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 8mA\left(1 - \frac{1.423}{4}\right)^2$$

$$\boxed{I_{DQ} = 3.32\ mA}$$

KVL to D-S loop gives,

$$-V_{DD} + I_D R_D - V_{DS} + I_D R_S = 0$$

$$V_{DS} = -V_{DD} + I_D(R_D + R_S)$$

$$= -20 + 3.32mA\,(2.7K + 1.8K)$$

$$\boxed{V_{DSQ} = -5.06\ V}$$

JFET Biasing (Graphical Analysis)

M 2.1

- Important relationships:

- $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ → Shockley's equation — (1)

→ $V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$

- $I_D = I_S$
- $I_G \approx 0A$

For JFET, a voltage is the controlling variable.

eg If $V_{GS} = \frac{V_P}{2}$ → $I_D = I_{DSS}\left(1 - \frac{V_P/2}{V_P}\right)^2 = (0.5)^2 I_{DSS}$

$= \frac{1}{4} I_{DSS}$.

if we choose $I_D = I_{DSS}/2$.

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}}\right)$$

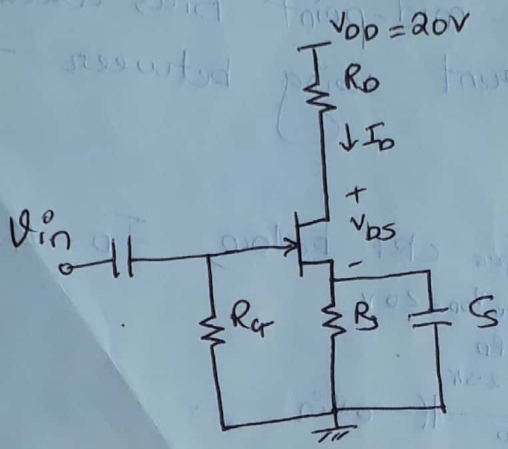
$$= V_P\left(1 - \sqrt{0.5}\right) = V_P(0.293) \approx 0.3V_P$$

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0

INDERJIT SINGH

JFET Biasing (Numericals):

1. In a self-bias n-channel JFET, $I_D = 1.5mA$, $V_{DS} = 10V$, JFET parameters are $I_{DSS} = 5mA$, and $V_p = -2V$., $V_{DD} = 20V$. Find the values of R_S and R_D.



Let $R_G = 1M\Omega$, $I_G \approx 0A$.

Soln:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)$$

$$V_{GS} = V_p\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) = (-2)\left(1 - \sqrt{\frac{1.5}{5}}\right)$$

$$\approx -1.4V.$$

$$V_{GS} = V_G - V_S = -V_S$$

$$V_S = 1.4V.$$

ie $V_S = I_D R_S$

$$R_S = \frac{1.4}{1.5mA} = 0.933K\Omega$$

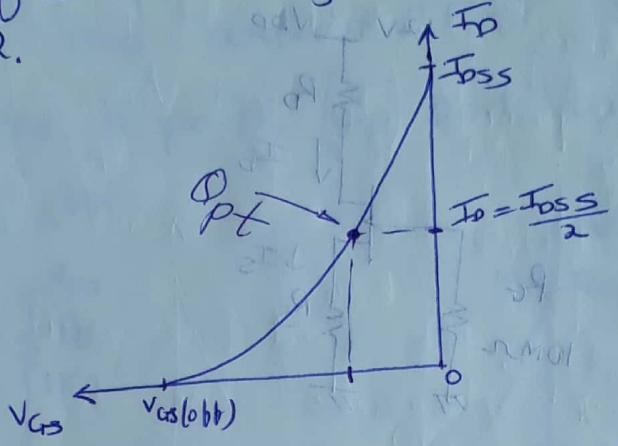
$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$R_D = \frac{V_{DD} - V_{DS} - I_D R_S}{I_D}$$

$$R_D = 5.7K\Omega$$

*Mid-point Bias: (Mid Point Biasing)

It is usually desirable to bias a JFET near the mid-point of its transfer characteristic curve where $I_D = I_{DSS}/2$.



- Under s/g conditions, midpt bias allows the max amt of drain current swing both I_{DSS} and 0.
- Using eqn (1) ie $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$

we can prove that $I_D \simeq \frac{I_{DSS}}{2}$ when $V_{GS} = \frac{V_{GS(off)}}{3.4}$.

ie $I_D = I_{DSS}\left(1 - \frac{V_{GS(off)}/3.4}{V_{GS(off)}}\right)^2 \simeq 0.5 I_{DSS}$.

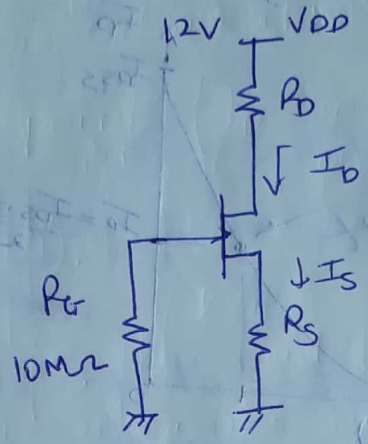
So, by selecting $V_{GS} = V_{GS(off)}/3.4$, we can get a mid-point bias in terms of I_D.

→ To set the drain voltage at midpoint ($V_D = V_{DD}/2$), select a value of R_D to produce the desired voltage drop.

{ Choose R_G arbitrarily large to prevent loading on the driving state in a cascaded amplifier ckt }

Ex: Find R_D and R_S to set up an approximate mid-point bias.

JFET parameters are $I_{DSS} = 12mA$ and $|V_{GS(off)}| = -3V$.



Soln: For midpoint bias,

$$V_D \approx \frac{V_{DD}}{2} \approx 6V.$$

Also, $I_D \approx \frac{I_{DSS}}{2} = 6mA.$

$$V_{GS} \approx \frac{V_{GS(off)}}{3.4} = \frac{-3}{3.4} = -0.882V.$$

$$\Rightarrow R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{0.882}{6mA} \approx 147\Omega$$

$$V_D = V_{DD} - I_D R_D$$

$$\rightarrow R_D = \frac{V_{DD} - I_D}{I_D}$$

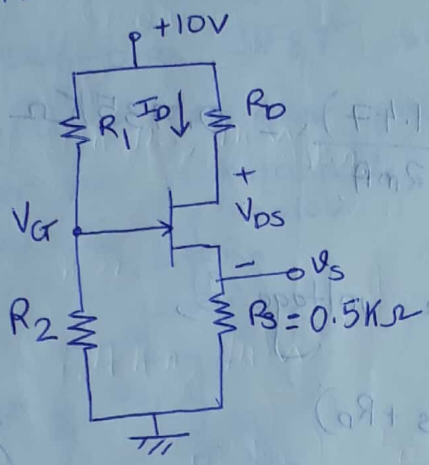
$$= \frac{(12 - 6)}{6mA}$$

$$R_D = 1K\Omega$$

2. Design an n-channel JFET with a voltage-divider bias circuit such that ~~Q-point~~ $I_D = 5mA$ and $V_{DS} = 5V$, with transistor parameters $I_{DSS} = 12mA$ and $V_P = -3.5V$

Solution:

Assume the JFET is biased in the saturation region.



- $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$
- $5mA = 12mA\left(1 - \frac{V_{GS}}{(-3.5)}\right)^2$
- $\frac{5}{12} = \left(1 + \frac{V_{GS}}{3.5}\right)^2$
- $\frac{V_{GS}}{3.5} = \sqrt{\frac{5}{12}} - 1$

$V_{GS} = 3.5\left[\sqrt{\frac{5}{12}} - 1\right] = -1.24V.$

- $V_S = I_D R_S = 5mA \times 0.5K\Omega = 2.5V.$

ie $V_G = V_{GS} + V_S = -1.24 + 2.5 = \underline{1.26V.}$

$$\cdot V_G = \left(\frac{R_2}{R_1+R_2}\right) V_{DD} \qquad \therefore R_1+R_2 = 100k\Omega.$$

$$\text{ie } 1.26 = \left(\frac{R_2}{100k}\right) 10$$

$$\text{ie } R_2 = \frac{1.26 \times 100k}{10}$$

$$R_2 = 12.6k\Omega, 1/4W$$

$$R_1+R_2 = 100k\Omega \text{ ---- Given}$$

$$R_1 = 87.4k\Omega, 1/4W$$

$$\cdot V_{DS} = V_{DD} - I_D(R_D) - I_D R_S$$

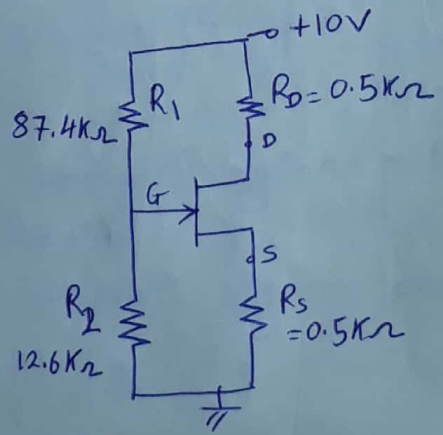
$$\Rightarrow R_D = \frac{V_{DD} - V_{DS} - I_D R_S}{I_D}$$

$$= \frac{10 - 5 - (5)_m 0.5k}{5mA}$$

$$R_D = 0.5k\Omega, 1/4W$$

(We also see that, $V_{DS} = 5V > V_{GS} - V_P = -1.24 - (-3.5) = 2.26V$. which shows that JFET is indeed in the saturation region)

Designed ckt is



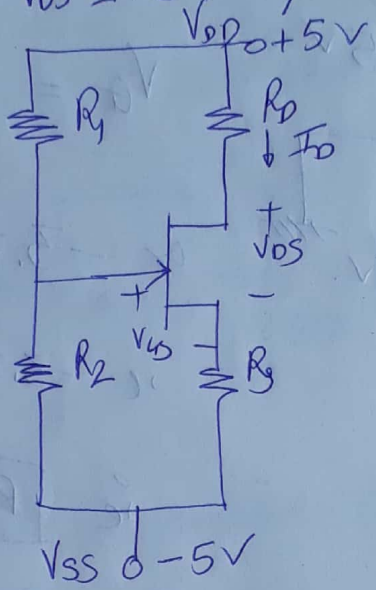
INDERJIT SINGH

16/10/19

* Design a nJFET circuit with a voltage-divider bias

$I_{DSS} = 12mA$, $V_P = -3.5V$, Let $R_1 + R_2 = 100K\Omega$

$I_D = 5mA$, $V_{DS} = 5V$, $R_S = 500\Omega$



Soln:- Assume nJFET is biased in saturation region

$$\text{ie } I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\text{ie } 5mA = 12mA\left(1 + \frac{V_{GS}}{3.5}\right)^2$$

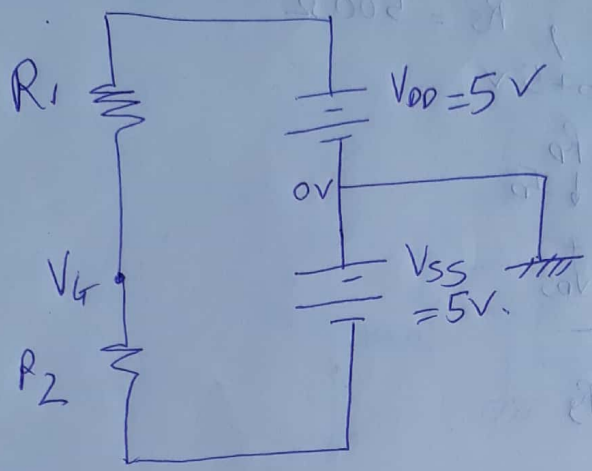
$$\rightarrow \boxed{V_{GS} = -1.24V}$$

. From circuit, $V_S = I_D R_S - 5$

$$V_S = 5mA \times 500 - 5 = -2.5V$$

$$\rightarrow V_G = V_{GS} + V_S = -1.24 - 2.5 = -3.74V$$

Also, $V_G = \left[\frac{R_2}{R_1+R_2}(V_{DD}+V_{SS}) - V_{SS}\right]$ how?



$$V_G = \frac{R_2}{R_1+R_2} \times (5+5) - 5$$

or $$-3.74 = \left(\frac{R_2}{R_1+R_2}\right) 10 - 5$$

i.e $$-3.74 = \frac{R_2 \times 10}{100K} - 5$$

ie $$\boxed{R_2 = 12.6K\Omega}$$

Since $R_1+R_2 = 100K\Omega \Rightarrow \underline{R_1 = 87.4K\Omega}$

Apply KVL around D-S loop,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S + V_{SS} = 0$$

$$R_D = \frac{V_{DD}+V_{SS}-V_{DS}-I_D R_S}{I_D} \simeq \frac{10 - V_{DS} - I_D R_S}{I_D}$$

$$R_D = \frac{10-5-5mA \times 500}{5mA} \Rightarrow \boxed{R_D = 0.5K\Omega}$$

Also, $V_{DS} > V_{GS} - V_P > -1.24 - (-3.5) > 2.26V$ & $V_{GS} > V_P$

∴ Given NJFET is indeed working in saturation region.

(1) Biasing the JFET for zero temperature drift

The variation of the drain current with temperature is shown in Fig. 3.23.

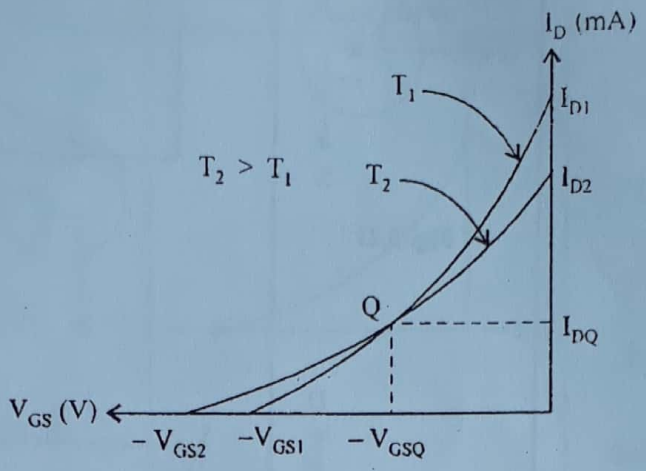


Fig. 3.23

There are two reasons for the drain current I_D to change with temperature.

(i) As temperature increases, the vibrations of ions in the channel increases. The vibrations will oppose the motion of electrons from drain to source. Hence drain current I_D decreases by 0.7%/°C.

(ii) As temperature increases, the width of the depletion region in channel decreases. Hence drain current I_D increases. It is found that the increase in I_D is equivalent to change of 2.2 mV/°C in V_{GS}.

For zero temperature drift biasing, the decrease in I_D with temperature should be equal to the increase in I_D with temperature.

Decrease in I_D with temperature = Increase in I_D with temperature

$$\Delta I_D \downarrow = g_m (\Delta V_{GS}) \uparrow$$

$$0.007\,|I_D| = g_m (0.0022)$$

$$\frac{|I_D|}{g_m} = 0.314$$

$$\frac{I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2}{g_{mo}\left(1-\frac{V_{GS}}{V_p}\right)} = 0.314$$

$$\frac{I_{DSS}\left(\frac{V_p - V_{GS}}{V_p}\right)}{\left(\frac{2\,I_{DSS}}{-V_p}\right)} = 0.314 \qquad \left(g_{mo} = \frac{2I_{DSS}}{|V_p|} = \frac{2I_{DSS}}{-V_p}\right)$$

$$V_p - V_{GS} = -0.63$$

$$|V_p| - |V_{GS}| = 0.63$$

This is the condition for biasing the JFET for zero temperature drift.

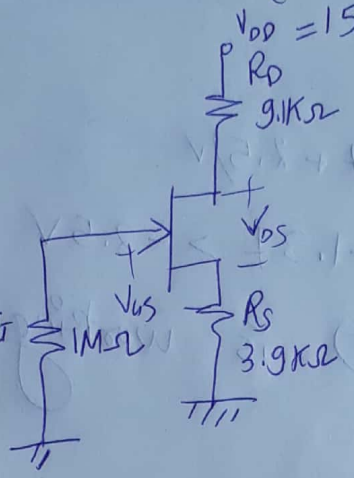
When the condition is satisfied,

(i) $$I_D = I_{DSS}\left(\frac{V_p - V_{GS}}{V_p}\right)^2$$

$$= I_{DSS}\left(\frac{0.63}{V_p}\right)^2$$

Numerical:-

Find I_D, V_{GS}, V_{DS} & determine region of operation for given device (Use zero temperature drift)



Sol?:- For Zero temperature biasing,

$$|V_P| - |V_{GS}| = 0.63$$

$$2.5 - |V_{GS}| = 0.63$$

$$|V_{GS}| = 1.87 \quad \text{ie} \quad \boxed{V_{GS} = -1.87\,V}$$

$$\rightarrow I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 7mA\left(1 - \frac{(-1.87)}{(-2.5)}\right)^2$$

$$\boxed{I_D = 0.44\,mA}$$

→ KVL to D-S loop,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\rightarrow V_{DS} = V_{DD} - I_D(R_D + R_S)$$

ie $V_{DS} = 15 - 0.44mA(9.1K\Omega + 3.9K\Omega)$

$$\boxed{V_{DS} = 9.28V}$$

As, $V_{DS} > (V_{GS} - V_P)$

ie $9.28V > (-1.87 + 2.5)V$

& Also, $V_{GS} > V_P$ ie $-1.87 > -2.5V$

The given device (JFET) is working in saturation mode of operation.

DC Analysis of Common Gate configuration:

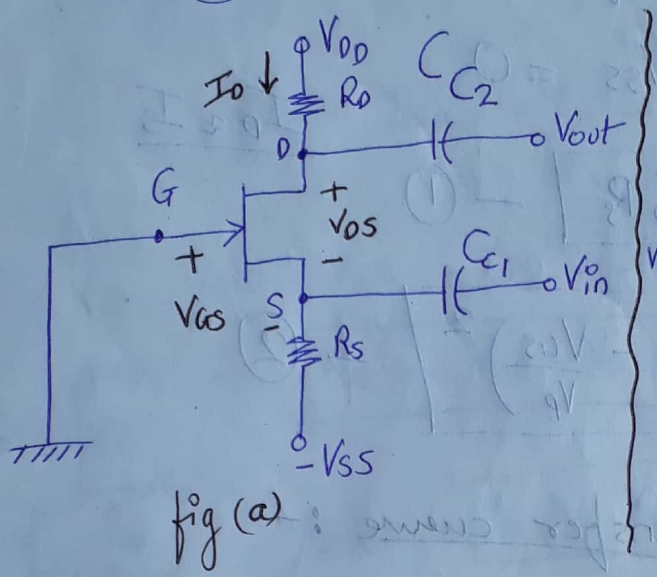


fig (a)

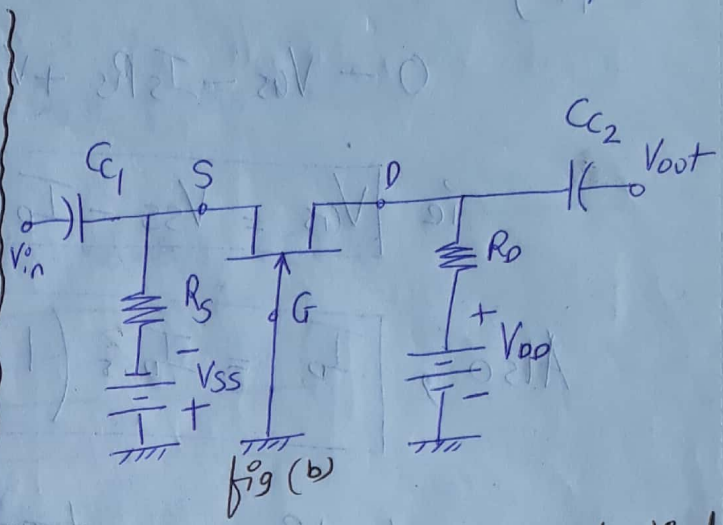


fig (b)

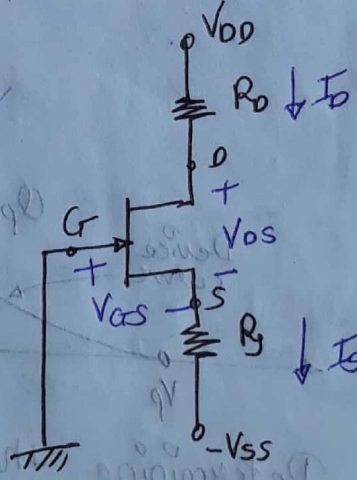
fig (a) & (b) are identical

Observations:-

- Gate terminal is grounded
- I/P signal is applied to the source terminal
- o/p signal is obtained at the drain terminal.
- For DC Analysis: ($f=0$); $X_C = \frac{1}{2\pi fC}$ $f=0$, $X_C=\infty$

  Since reactance offered by capacitors is ∞, we replace them by open-circuit.

- Circuit becomes:-



ckt (c)

Apply KVL to G-S loop of ckt (c),

$$0 - V_{GS} - I_S R_S + V_{SS} = 0$$

$I_D \approx I_S$

ie $\boxed{V_{GS} = V_{SS} - I_D R_S}$ — (1)

Also, $\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$ — (2)

• DC Load Line on transfer curve :-

Load Line co-ordinates:-

→ In eqn (1), Put $I_D = 0 \Rightarrow V_{GS} = V_{SS}$

ie 1st point $\equiv (V_{SS}, 0)$

→ In eqn (1), Put $V_{GS} = 0 \Rightarrow 0 = V_{SS} - I_D R_S$

$I_D = \frac{V_{SS}}{R_S}$ ie 2nd point $\equiv \left(0, \frac{V_{SS}}{R_S}\right)$

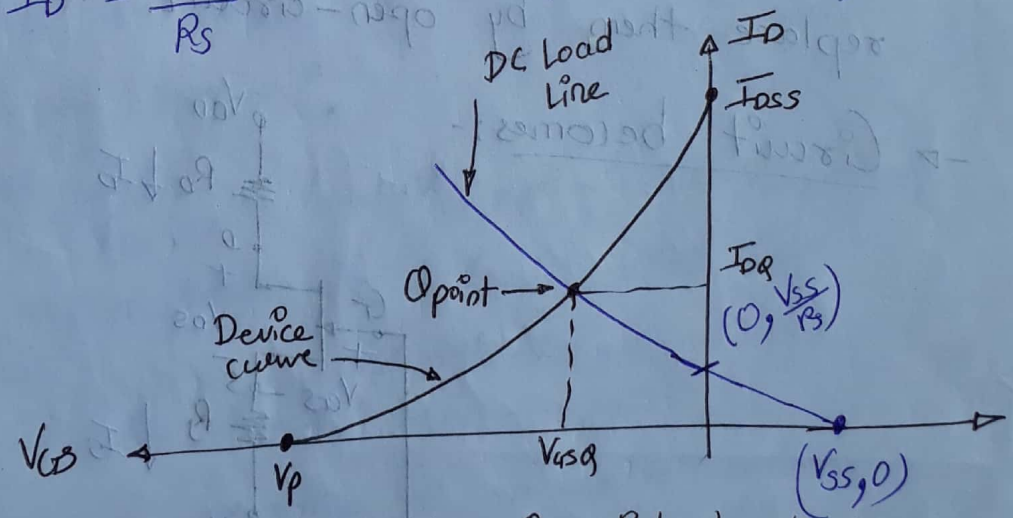


fig (d): Determining the Q-point of ckt (c)

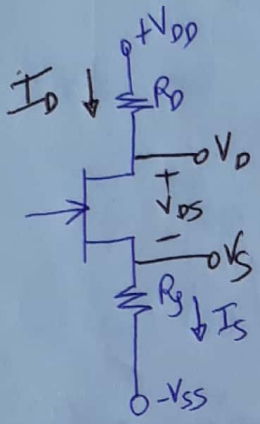
→ Applying KVL to D-S loop of ckt c, we get

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S + V_{SS} = 0$$

$I_D \simeq I_S$

$$V_{DD} + V_{SS} - V_{DS} - I_D (R_D + R_S) = 0$$

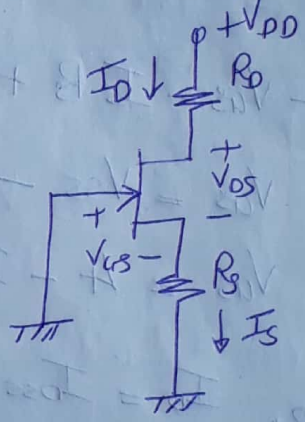
ie $\boxed{V_{DS} = V_{DD} + V_{SS} - I_D (R_D + R_S)}$



Now, $\boxed{V_D = V_{DD} - I_D R_D}$

$V_S - I_D R_S + V_{SS} = 0 \Rightarrow \boxed{V_S = -V_{SS} + I_D R_S}$

If $V_{SS} = 0$ in ckt ©, we have

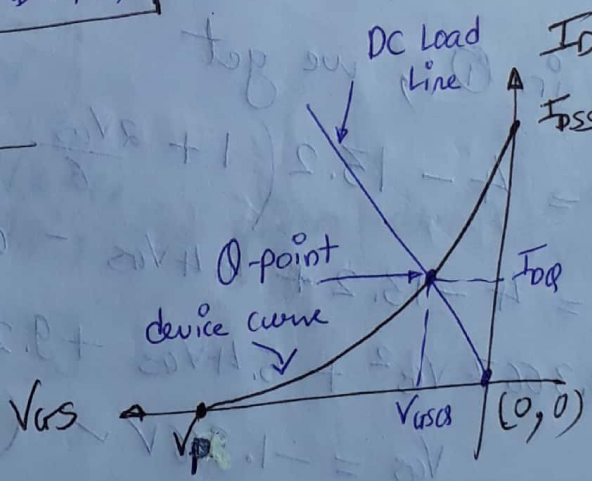


$V_G = 0$; $V_S = I_D R_S$

ie $\boxed{V_{GS} = -I_D R_S}$

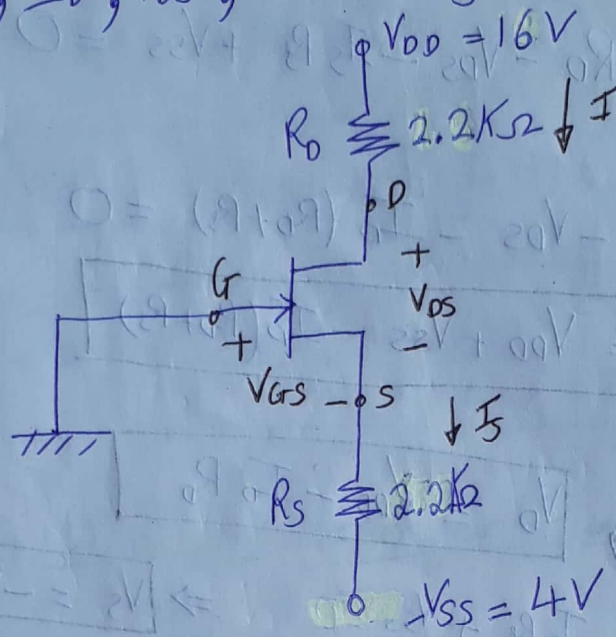
ie $\boxed{V_{DS} = V_{DD} - I_D (R_D + R_S)}$

Load line becomes:



Numerical :

Find V_{GS}, I_D, V_{DS}, and V_D for the circuit below :-



$I_{DSS} = 6\,mA$

$V_P = -6V$

Soln:- KVL to G-S loop,

$$0 - V_{GS} - I_S R_S + V_{SS} = 0$$

$I_D = I_S$

$$V_{GS} = V_{SS} - I_D R_S$$

$$\rightarrow V_{GS} = 4 - I_D(2.2K) \quad -(1)$$

Also, $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 6mA\left(1 + \frac{V_{GS}}{6}\right)^2 \quad -(2)$

Put (2) in (1), we get

$$\rightarrow V_{GS} = 4 - 13.2\left(1 + \frac{2V_{GS}}{6} + \frac{V_{GS}^2}{36}\right)$$

$$V_{GS} = 4 - 13.2 - 4.4V_{GS} - 0.3667V_{GS}^2$$

ie $0.3667V_{GS}^2 + 5.4V_{GS} + 9.2 = 0$

$V_{GS} = -1.966V$ ✓ (We select $-1.966V$ since $V_{GS} < V_P$)

or

$-12.75V$ ✗

$V_{GS} = -1.966V$

→ $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ ---- (Assume that transistor is in saturatn region)

$= 6mA\left(1 - \frac{(-1.966)}{(-6)}\right)^2$

$I_D = 2.71\ mA$

KVL to D-S loop,

$V_{DD} - I_D R_D - V_{DS} - I_S R_S + V_{SS} = 0$

$I_D = I_S$

ie $V_{DD} + V_{SS} - V_{DS} - I_D(R_D + R_S) = 0$

ie $V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$

$= 16 + 4 - 2.71mA(2.2K + 2.2K)$

$V_{DS} = 8.076\ V$

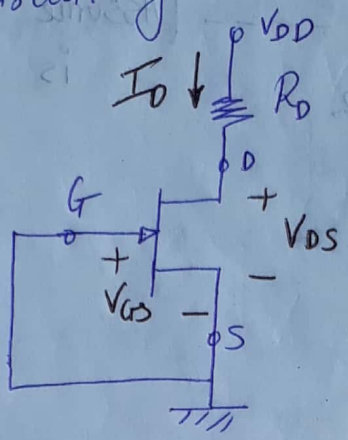
→ $V_D = V_{DD} - I_D R_D$

$= 16 - 2.71mA \times 2.2K\Omega$

$V_D = 10.038\ V$

→ Since $V_{DS} > (V_{GS} - V_P)$, the given device (JFET) is working in saturation region

1. Draw DC load line and mark the Q-point for the circuit given below:-

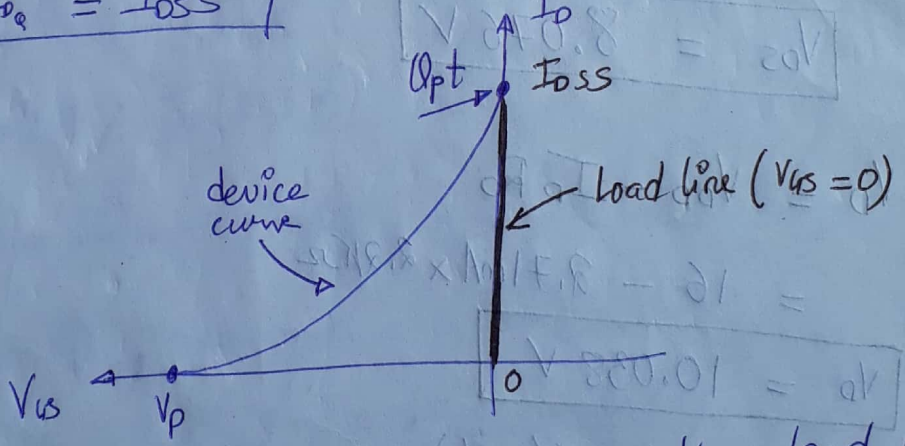


Soln:- Since gate & source terminals are shorted to ground,

$\rightarrow \boxed{V_{GS_Q} = 0}$

ie $I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = I_{DSS}(1-0)$

$\boxed{I_{D_Q} = I_{DSS}}$



→ The transfer curve of JFET cross the load line at I_{DSS}.

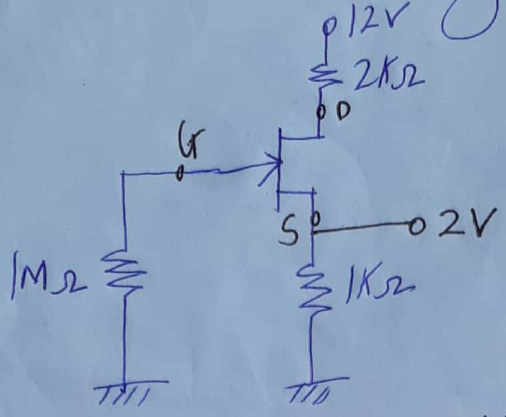
KVL at D-S loop, $V_{DD} - I_D R_D - V_{DS} = 0$

$\boxed{V_{DS} = V_{DD} - I_D R_D}$

$\boxed{V_S = 0}$; $\boxed{V_D = V_{DS}}$

. Determine the operating region for circuits below:- 07

a)



JFET in the

$I_{DSS} = 7mA$

$V_P = -4V$

Soln: From circuit, $V_S = 4V$

$V_G = 0$;

$V_S = I_S R_S = I_D R_S$

ie $V_S = I_D R_S \Rightarrow I_D = \frac{V_S}{R_S} = \frac{2V}{1K\Omega}$

$\rightarrow \boxed{I_D = 2mA}$

KVL to D-S loop

ie $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 12 - 2mA(2K + 1K)$

$= 12 - 6 = 6V$

ie $\boxed{V_{DS} = 6V}$; $V_{GS} = V_G - V_S$

$= 0 - 2$

$\boxed{V_{GS} = -2V}$

i) $V_{GS} < V_P$ ie $(-2) < (-4)$

and ii) $V_{DS} > V_{GS} - V_P$

ie $6V > -2 - (-4)$

$6V > 2V$

Since, both the cond's are satisfied, given device JFET in the circuit is operating in "saturation" region