Design Rules for NMOS and CMOS

- Design Rules
- Stick Diagrams
- Layout Diagram
- Examples

Darshana Sankhe

Design Rules: Introduction

- Design rules are a set of geometrical specifications that dictate the design of the layout
- Layout is top view of a chip
- Design process are aided by stick diagram and layout
- Stick diagram gives the placement of different components and their connection details
- But the dimensions of devices are not mentioned
- Circuit design with all dimensions is Layout

Design Rules: Introduction

- Fabrication process needs different masks, these masks are prepared from layout
- Layout is an Interface between circuit designer and fabrication engineer
- Layout is made using a set of design rules.
- Design rules allow translation of circuit (usually in stick diagram or symbolic form) into actual geometry in silicon wafer
- These rules usually specify the minimum allowable line widths for physical objects on-chip
- Example: metal, polysilicon, interconnects, diffusion areas, minimum feature dimensions, and minimum allowable separations between two such features.

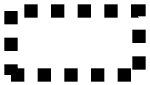
NEED FOR DESIGN RULES

- Better area efficiency
- Better yield
- Better reliability
- Increase the probability of fabricating a successful product on Si wafer

If design rules are not followed:

- Functional or non-functional circuit.
- Design consuming larger Si area.
- The device can fail during or after simulation.

Colour Codes :

Layer	Color	Representation
N+ Active	Green	
P+ Active	Yellow	
PolySi	Red	
Metal 1	Blue	
Metal 2	Magenta	
Contact	Black	X
Buried contact	Brown	X
Via	Black	X
Implant	Dotted yellow	
N-Well	Dotted Green/Black	

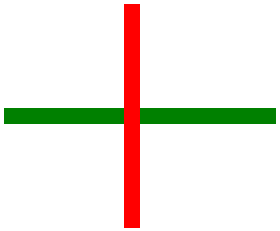
Stick Diagrams :

- A stick diagram is a symbolic representation of a layout.
- In stick diagram, each conductive layer is represented by a line of distinct color.
- Width of line is not important, as stick diagrams just give only wiring and routing information.
- Does show all components/vias, relative placement.
- Does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries.

Stick Diagrams: Basic Rules

- Poly crosses diffusion forms transistor
- Red (poly) over Green(Active), gives a FET.

L:W



nFET/
nMOS

- Aspect Ratio

L:W

pFET/pMOS

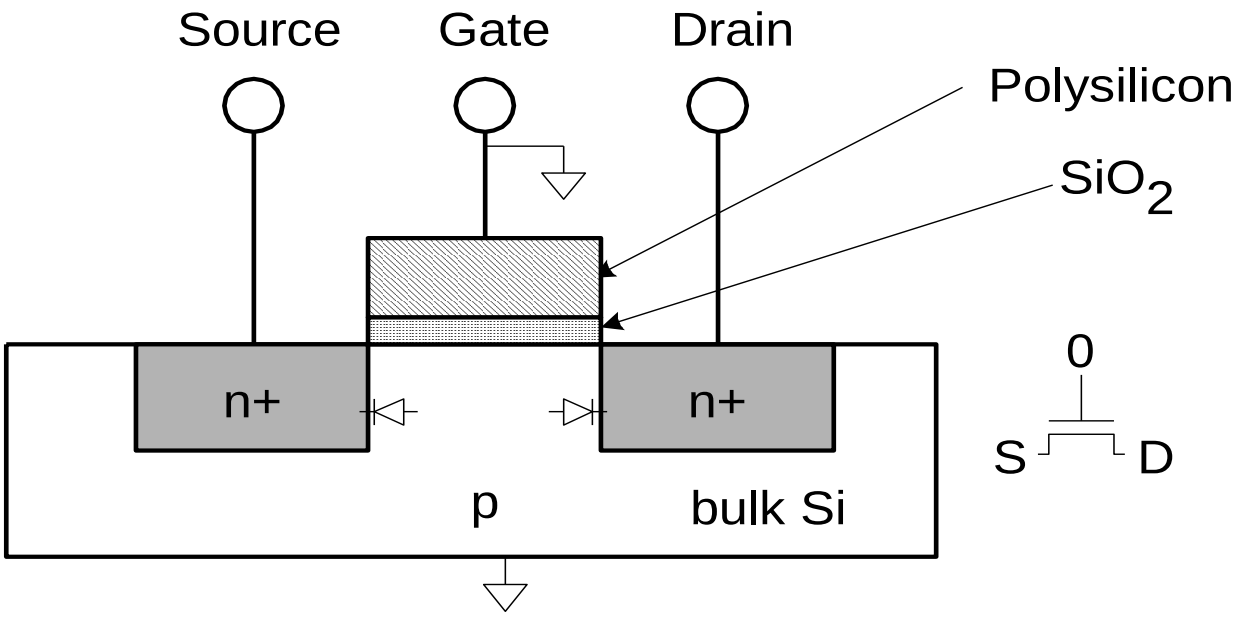
Stick Diagrams: Basic Rules

- Blue may cross over red or green, without connection.
- Connection between layers is specified with **X**.
- Metal lines on different layer can cross one another, connections are done using via.

Stick Diagrams(NMOS): Basic Steps

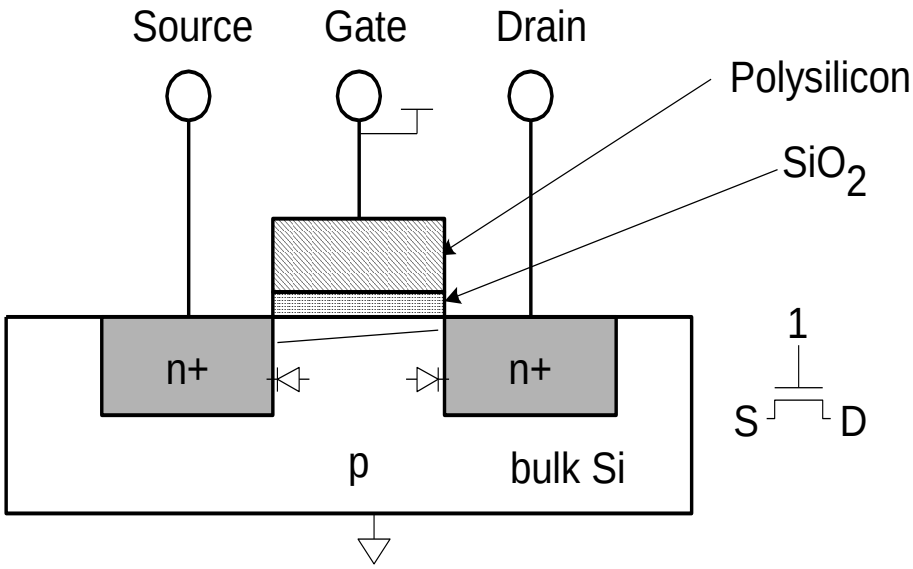
- Normally, the first step is to draw two parallel metal (blue) V_{DD} and GND rails.
- There should be enough space between them for other circuit elements.
- Next, Active (Green) paths must be drawn for required transistors.
- Do not forget to mark contacts as **X**, wherever required.
- Remember, Poly (Red) crosses Active (Green/yellow), where transistor is required.
- For depletion mode FET, draw required implants (yellow).
- Label each transistor with L:W ratio.

Enhancement-Mode MOSFET :



Enhancement-Mode MOSFET :

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON



Inverter Using MOSFET

- Enhancement-Mode MOSFETs act as switches.
- They are switched OFF, when the input to gate is low.
- So, they can be used to pull the output down.
- Now, for pull-up, we can use a resistor.
- But resistors consume larger area.
- Another alternative is using MOSFET as pull-up.

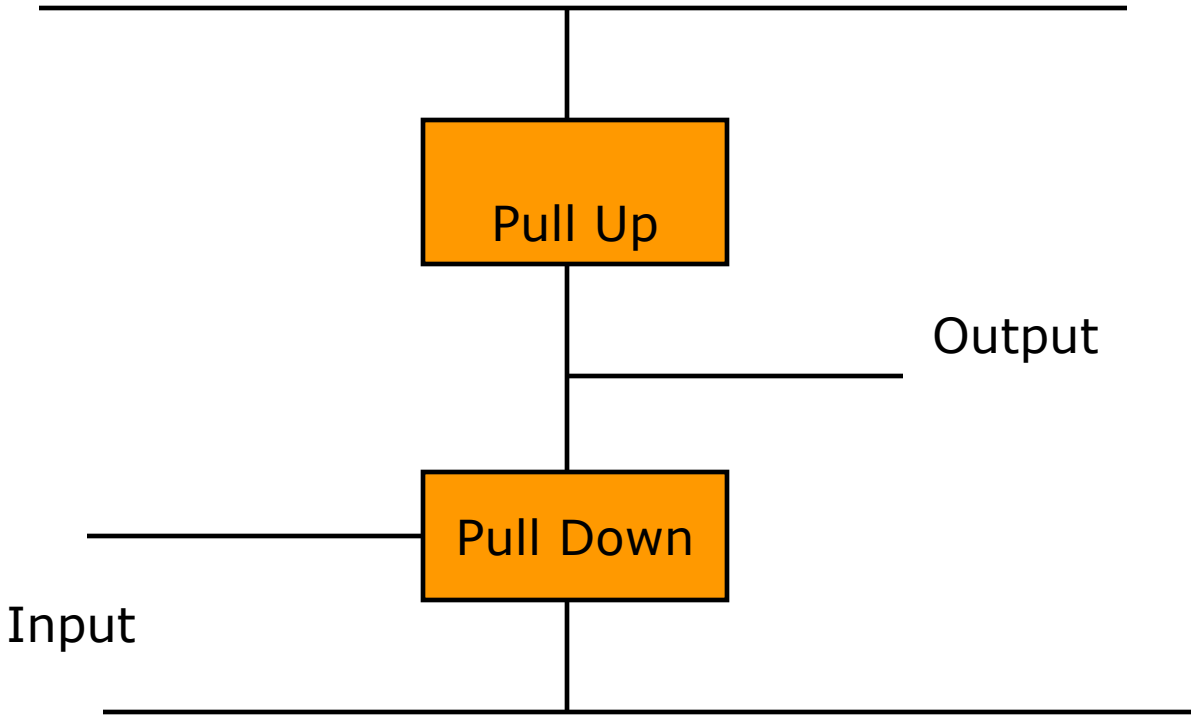
Inverter Using MOSFET

- The pull-up MOSFET can be Enhancement-mode or Depletion mode.
- Enhancement-mode as pull-up:
  - To use Enhancement-mode FET as active load, the gate should be connected to a separate gate bias voltage.
  - Vo(max) = VDD - Vth

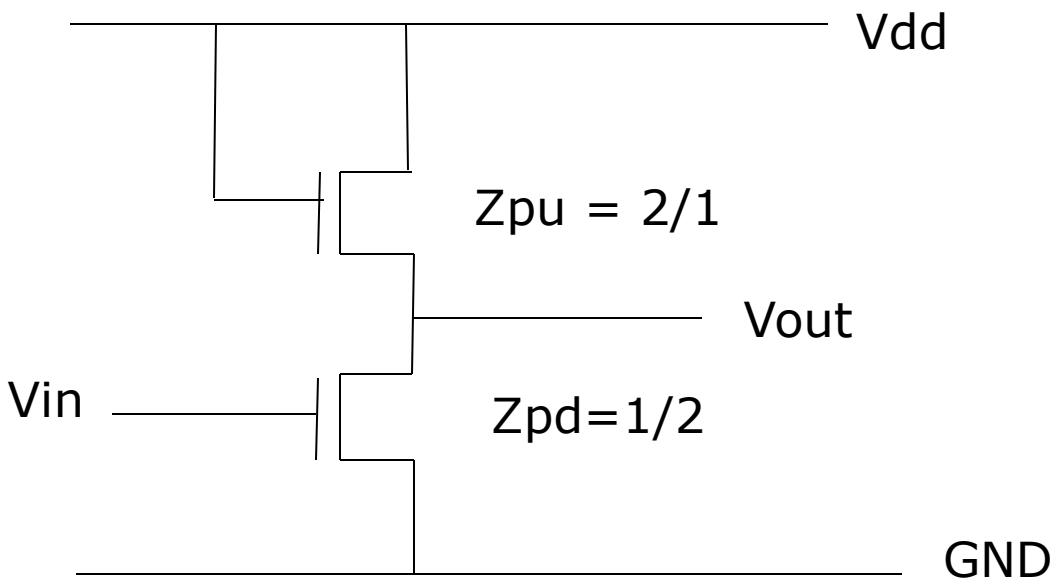
Inverter Using MOSFET

- Depletion mode as pull-up:
  - Depletion-Mode FET has a channel with zero gate-bias.
  - They will not turn-off until sufficient reverse bias is applied to its gate.
  - To be used as a load, the gate should be connected to source.
  - Vo(max) = VDD

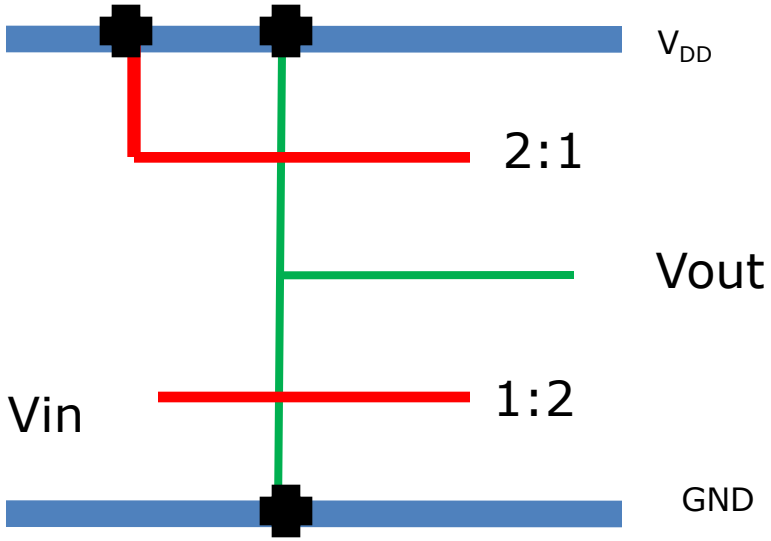
Inverter Using MOSFET



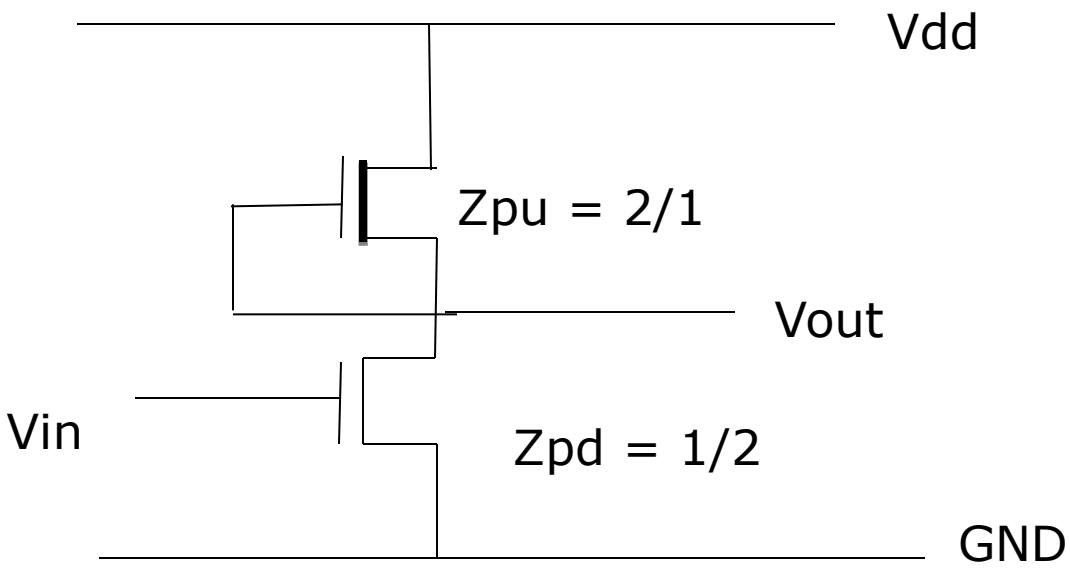
NMOS Inverter: Enhancement load



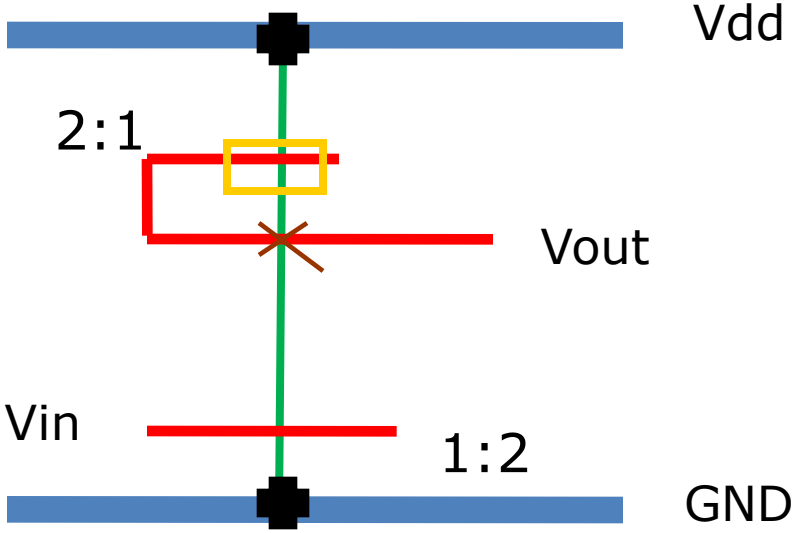
NMOS Inverter: Enhancement load (Stick diagram)



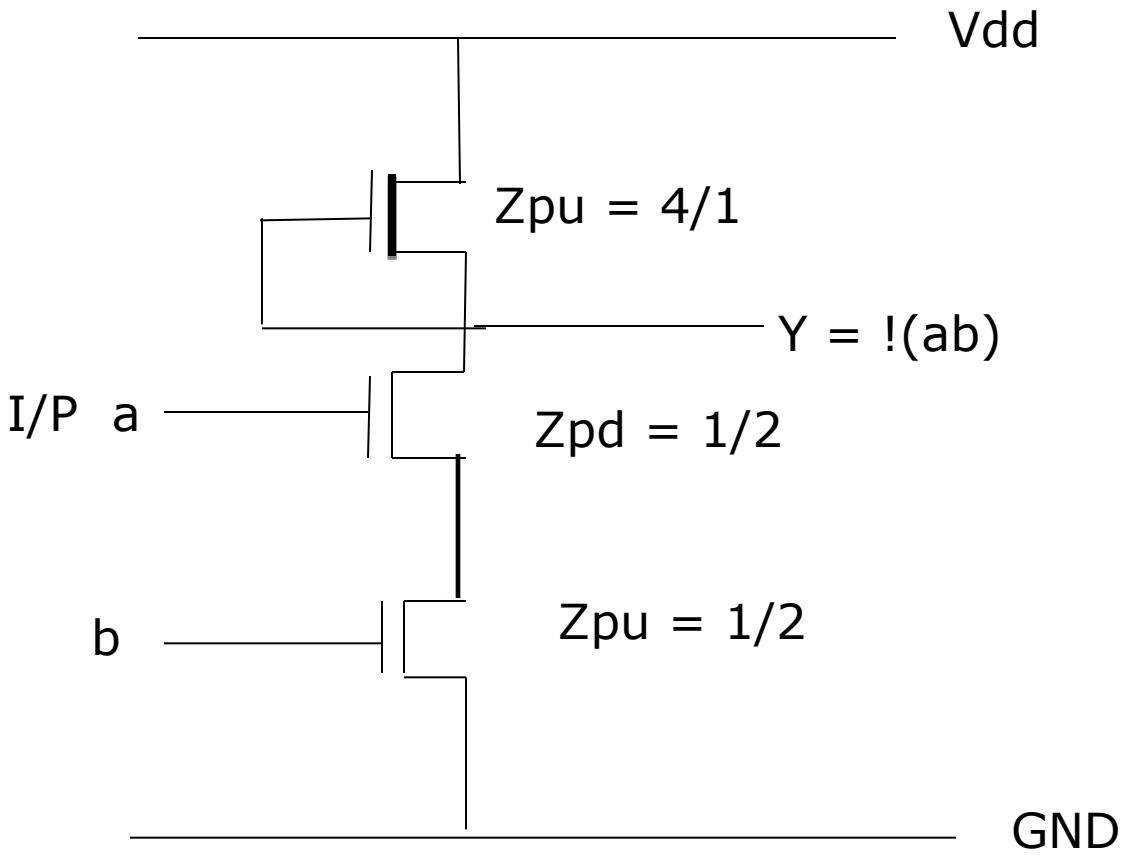
NMOS Inverter: Depletion load



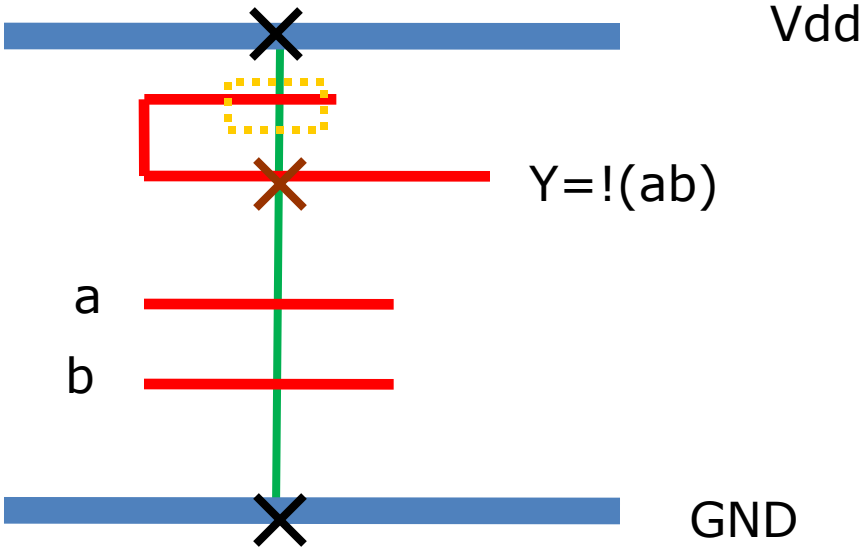
NMOS Inverter: Depletion load (Stick Diagram)



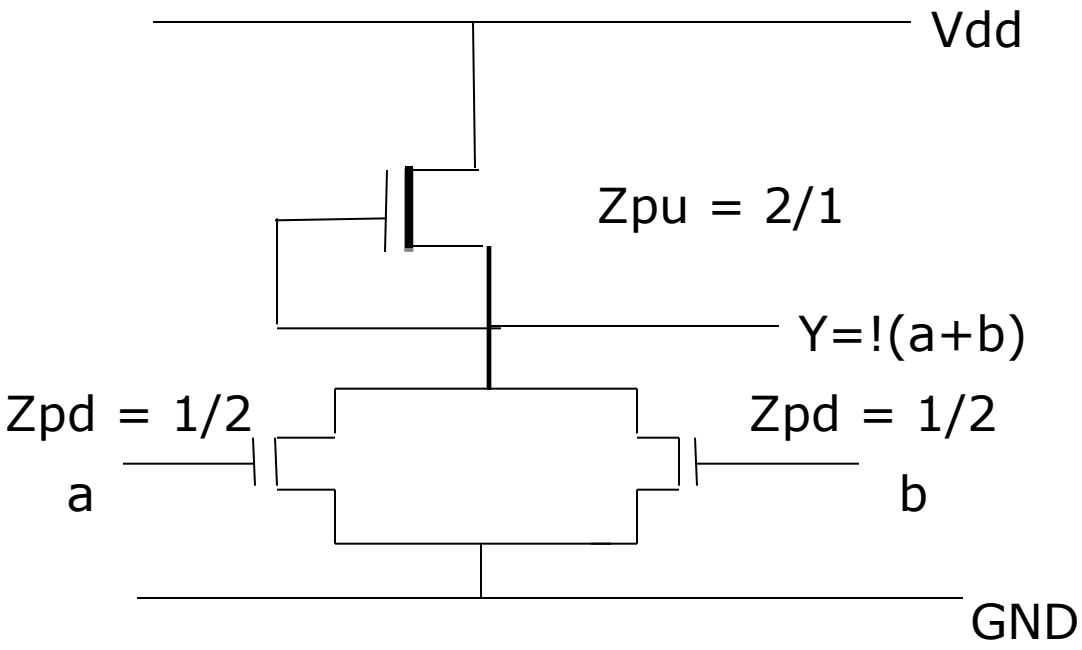
NMOS 2 I/P NAND Gate :



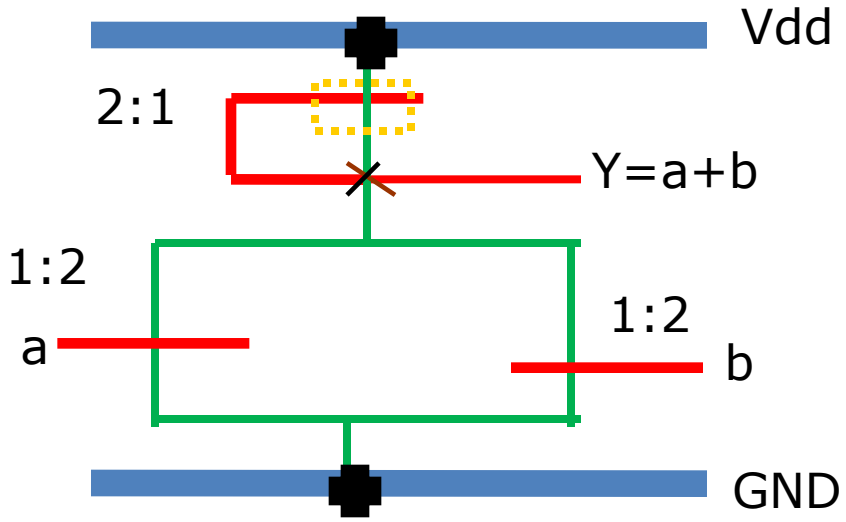
NMOS NAND (Stick Diagram) :



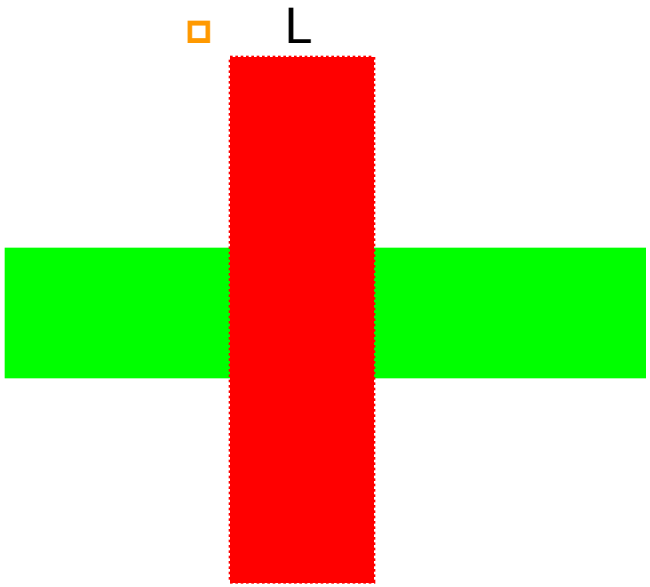
NMOS 2 I/P NOR Gate :

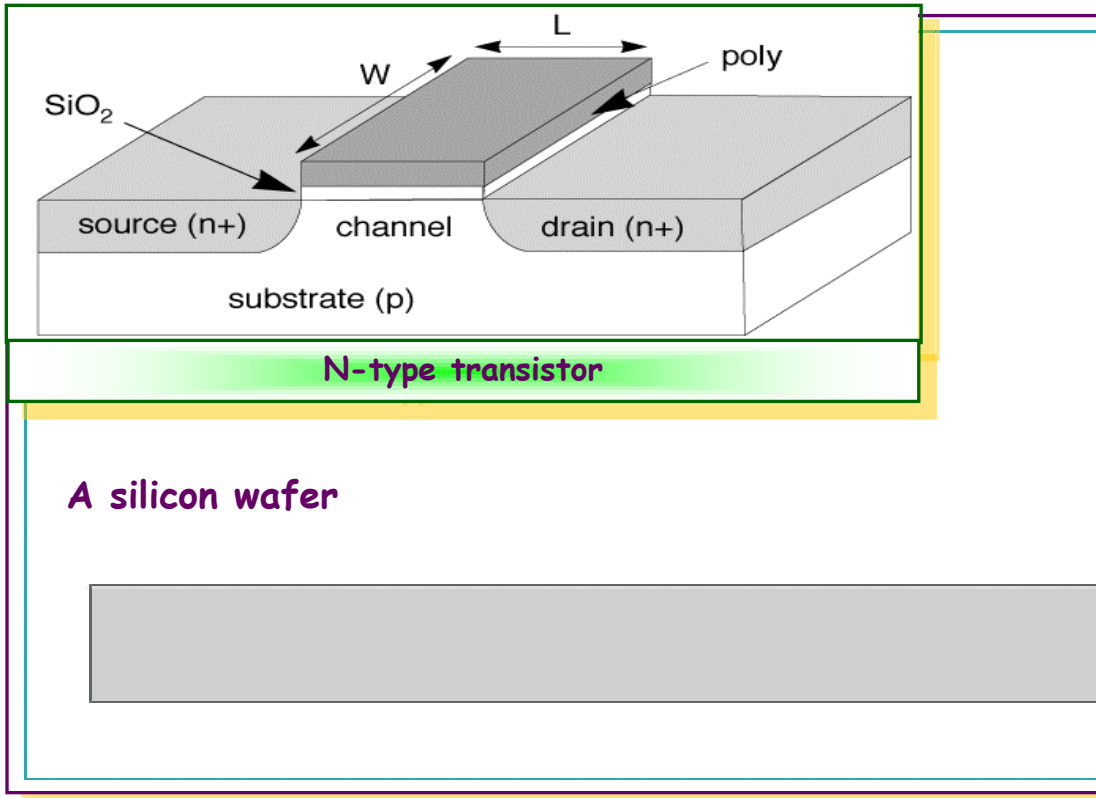


NMOS NOR (Stick Diagram)



MOSFET


L


L
W
poly
SiO_2
source (n+)
channel
drain (n+)
substrate (p)
N-type transistor
A silicon wafer

Aspect Ratio For Pull-up and Pull-down

- The size of a MOSFET depends on the reference inverter design.
- The reference inverter for nMOS logic design is the inverter with depletion mode load.
- Z_{PD} = Aspect Ratio of pull-down= L_{PD}/W_{PD}
- Z_{PU} = Aspect Ratio of pull-up= L_{PU}/W_{PU}
- The ratio of aspect ratio of Pull-up and Pull-down is known as Inverter Ratio i.e. $R_{inv} = Z_{PU} / Z_{PD}$
- When we draw a stick diagram, inverter ratio should be mentioned for that gate.
- When a we draw a stick diagram, aspect ratio should be mentioned for all the MOSFETS.

Aspect Ratio For Pull-up and Pull-down

- For example, if we say, the reference design has R_{inv} = 4:1, then, ratio of effective Z_{PU} and effective $Z_{PD,}$ should be equal to 4:1.
- $R_{channel} = (L/W)R_{sc}$
- Therefore:
  - if MOSFETs are connected in series, the effective $L/W = (L/W)_1+(L/W)_2+\ldots$
  - if MOSFETs are connected in parallel, the effective $L/W = (L/W)_{1=} (L/W)_2$

Aspect Ratio For Pull-up and Pull-down

For NMOS:

- There are two values of R_{inv}, that are sufficient for all NMOS basic gates:
  - R_{inv} = 4:1
    - To save space.
  - R_{inv} = 8:1
    - When input is taken from a pass transistor.

Inverter Ratio for NMOS Gates :

Gates	R_{inv}	Z_{PU}	Z_{PD}
Inverter	4	2:1	1:2
		4:1	1:1
	8	8:1	1:1
		4:1	1:2
		2:1	1:4
NAND (2 I/P)	4	4:1	1:2 (Each)
		2:1	1:4 (Each)
NOR (2 I/P)	4	2:1	1:2 (Each)
		4:1	1:1 (Each)

NMOS NAND and NOR :

NMOS NAND

- Two nmos in series.
- Gate delay and area increases with increase in no of inputs.
- Length also increases with increase in no of input.
- NMOS NAND is slower for same no of inputs and power dissipation.

NMOS NOR

- Two nmos in parallel.
- NOR works quite well for any no of inputs.
- Width is proportional to number of inputs.
- NMOS NOR is faster for same no of inputs and power dissipation.

Types of Layout Design Rules

- Industry Standard: Micron Rule
- λ Based Design Rules

Types of Design Rules (Contd…)

- Industry Standard: Micron Rule
  - All device dimensions are expressed in terms of absolute dimension(μm/nm)
  - These rules will not support proportional scaling

Types of Design Rules (Contd…)

- λ Based Design Rules :
  - Developed by Mead and Conway.
  - All device dimensions are expresses in terms of a scalable parameter λ.
  - λ = L/2; L = The minimum feature size of transistor
  - L = 2 λ
  - These rules support proportional scaling.
  - They should be applied carefully in sub-micron CMOS process.

Types of Design Rules (Contd…)

- λ Based Design Rules

  - In MOS, the minimum feature size of Tr is:

    (L/W)n = 1/1 = 2 λ/2 λ

    Active area = L*W = 4 λ^2

  - In CMOS, the minimum feature size of Tr is:

    (L/W)n = 1/1.5 = 2 λ/3 λ

    Active area = L*W = 6 λ^2

Design Rules

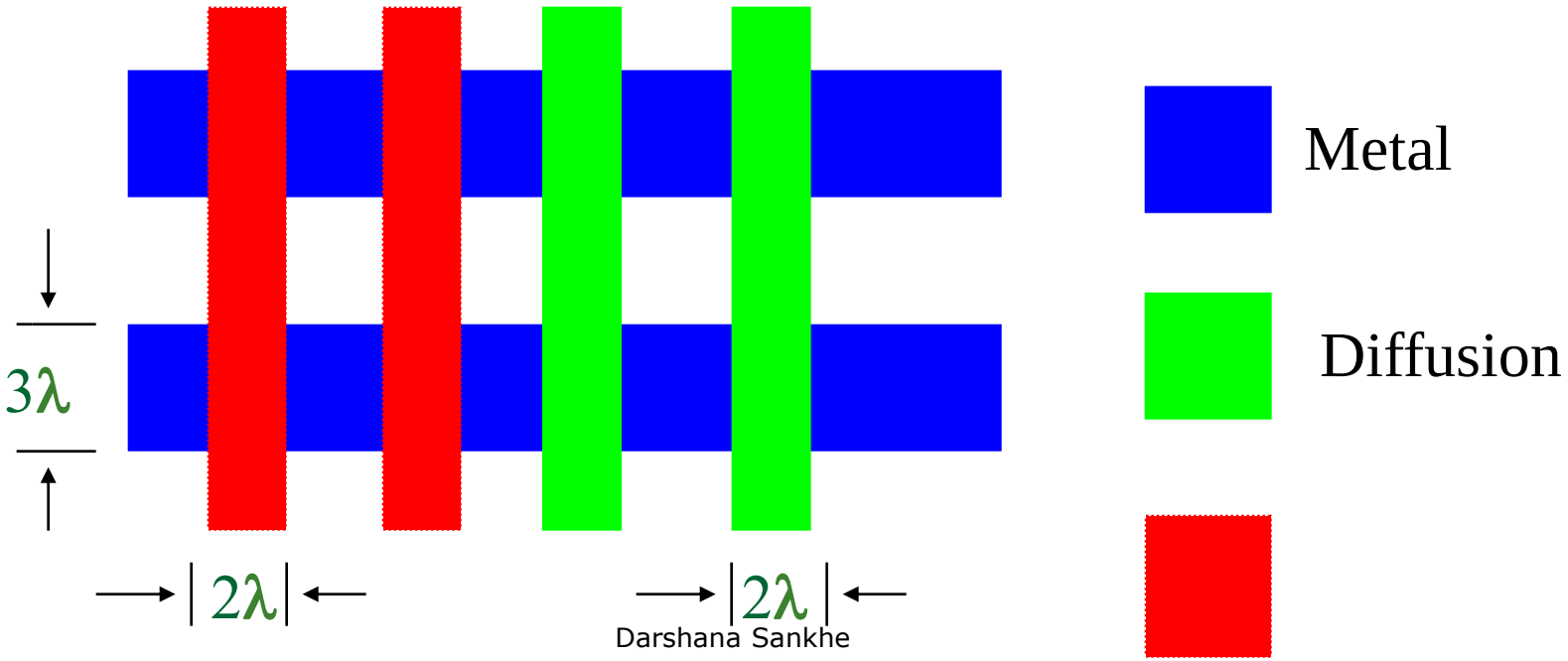
- Minimum length or width of a feature on a layer is **2λ**
  - To allow for shape contraction
- Minimum separation of features on a layer is 2λ
  - To ensure adequate continuity of the intervening materials.

Design Rules :

- Two Features on different mask layers can be misaligned by a maximum of 2λ on the wafer.
- If the overlap of these two different mask layers can be catastrophic to the design, they must be separated by at least 2λ
- If the overlap is just undesirable, they must be separated by at least λ

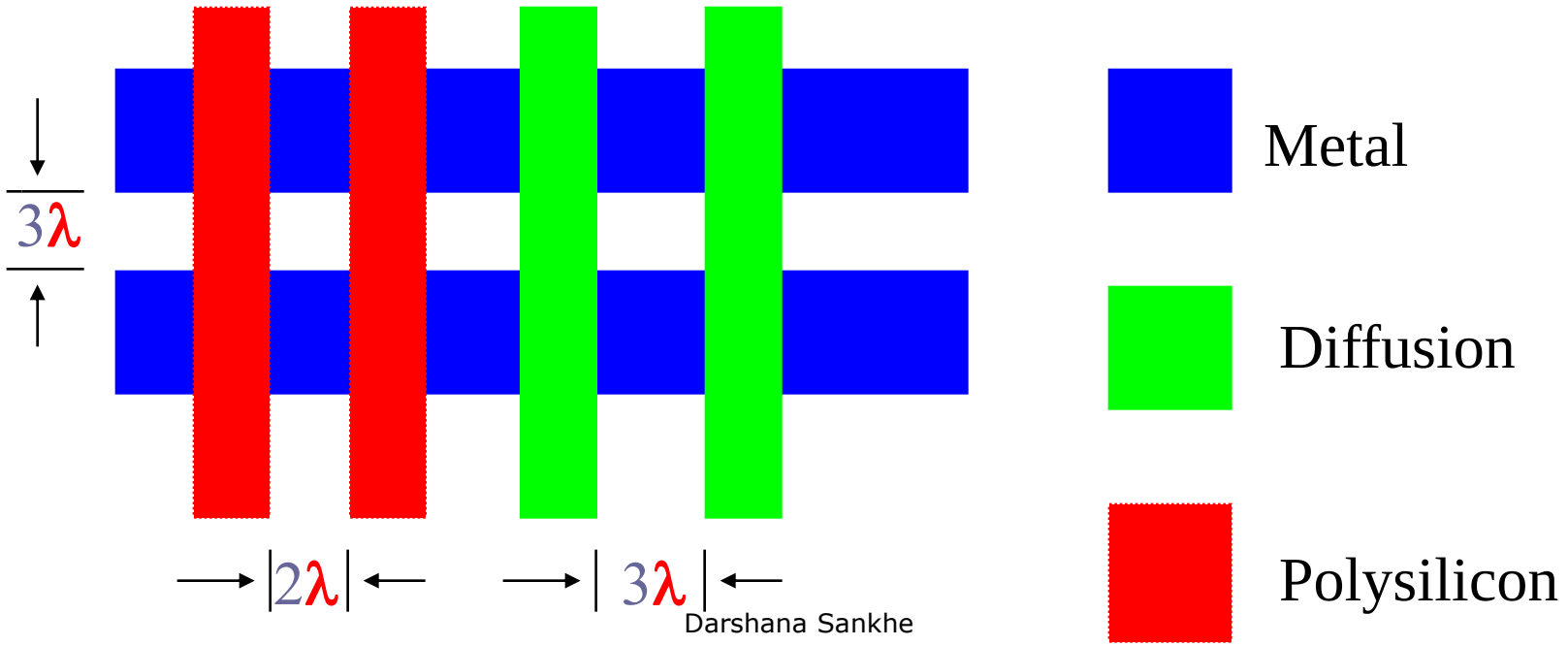
Design Rules: NMOS

- Minimum width of PolySi and diffusion line **2λ**
- Minimum width of Metal line **3λ** as metal lines run over a more uneven surface than other conducting layers to ensure their continuity



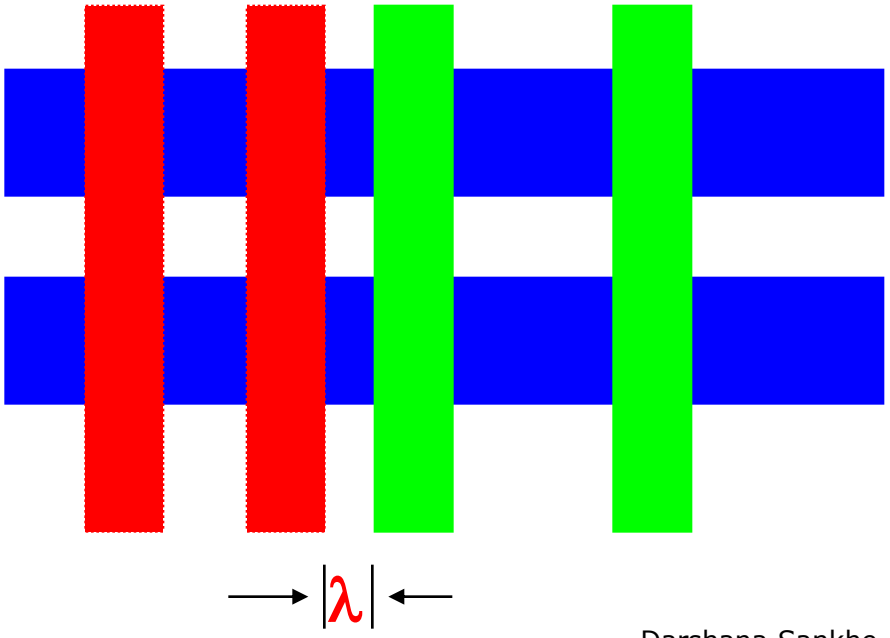
Design Rules: NMOS

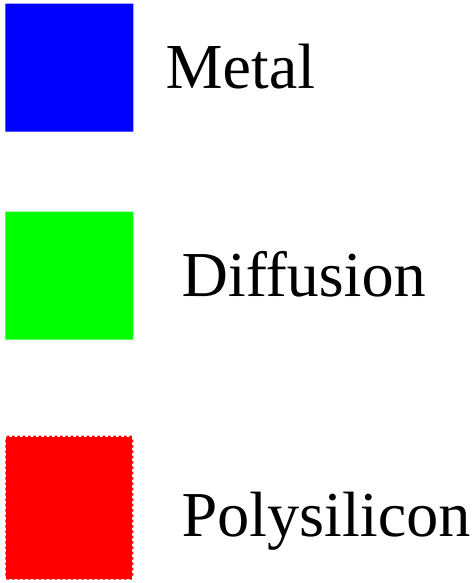
- **PolySi – PolySi spacing 2λ**
- **Metal - Metal spacing 3λ**
- **Diffusion – Diffusion spacing 3λ To avoid the possibility of their associated regions overlapping and conducting current**



Design Rules: NMOS

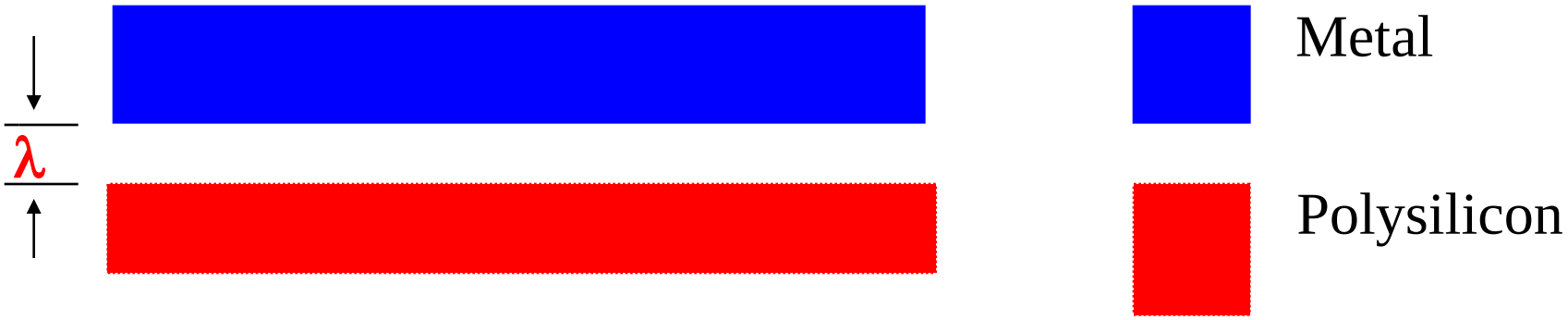
- **Diffusion – PolySi spacing λ To prevent the lines overlapping to form unwanted capacitor.**
- **Metal lines can pass over both diffusion and polySi without electrical effect. Where no separation is specified, metal lines can overlap or cross.**





Design Rules: NMOS

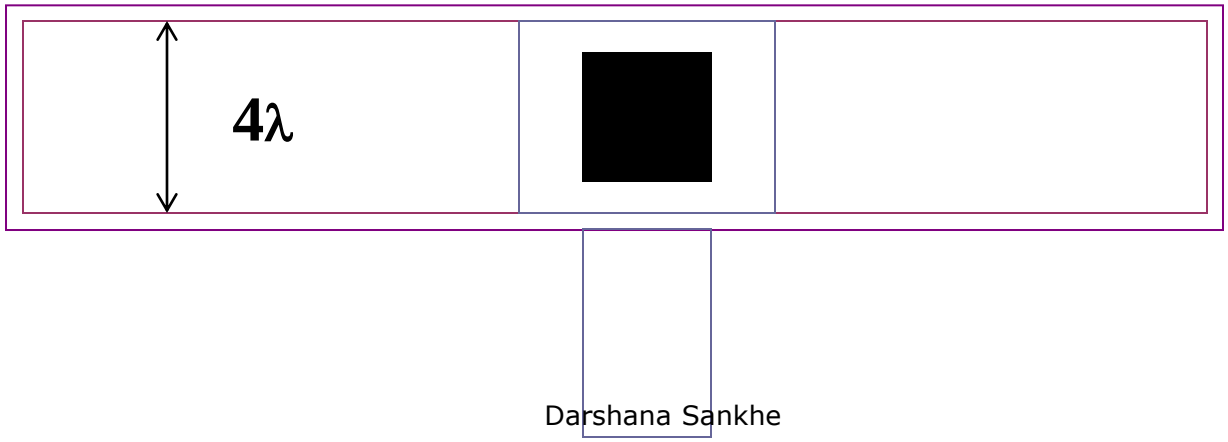
- **Metal lines can pass over both diffusion and polySi without electrical effect**
- **It is recommended practice to leave λ between a metal edge and a polySi or diffusion line to which it is not electrically connected**



Contact Cut :

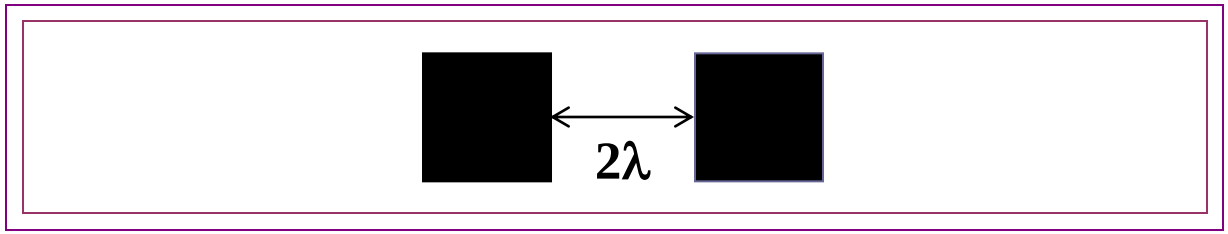
- **Metal connects to polySi/diffusion by contact cut.**
- **Contact area: 2λ*2λ**

- **Metal and polySi or diffusion must overlap this contact area by λ so that the two desired conductors encompass the contact area despite any mis-alignment between conducting layers and the contact hole**



Contact Cut

- Contact cut – contact cut: 2λ apart
- Why? To prevent holes from merging.



Design Rules: NMOS

- Minimum diff width 2λ
- Minimum poly width 2λ
- Minimum metal width 3λ
- poly-poly spacing 2λ

- diff-diff spacing 3λ

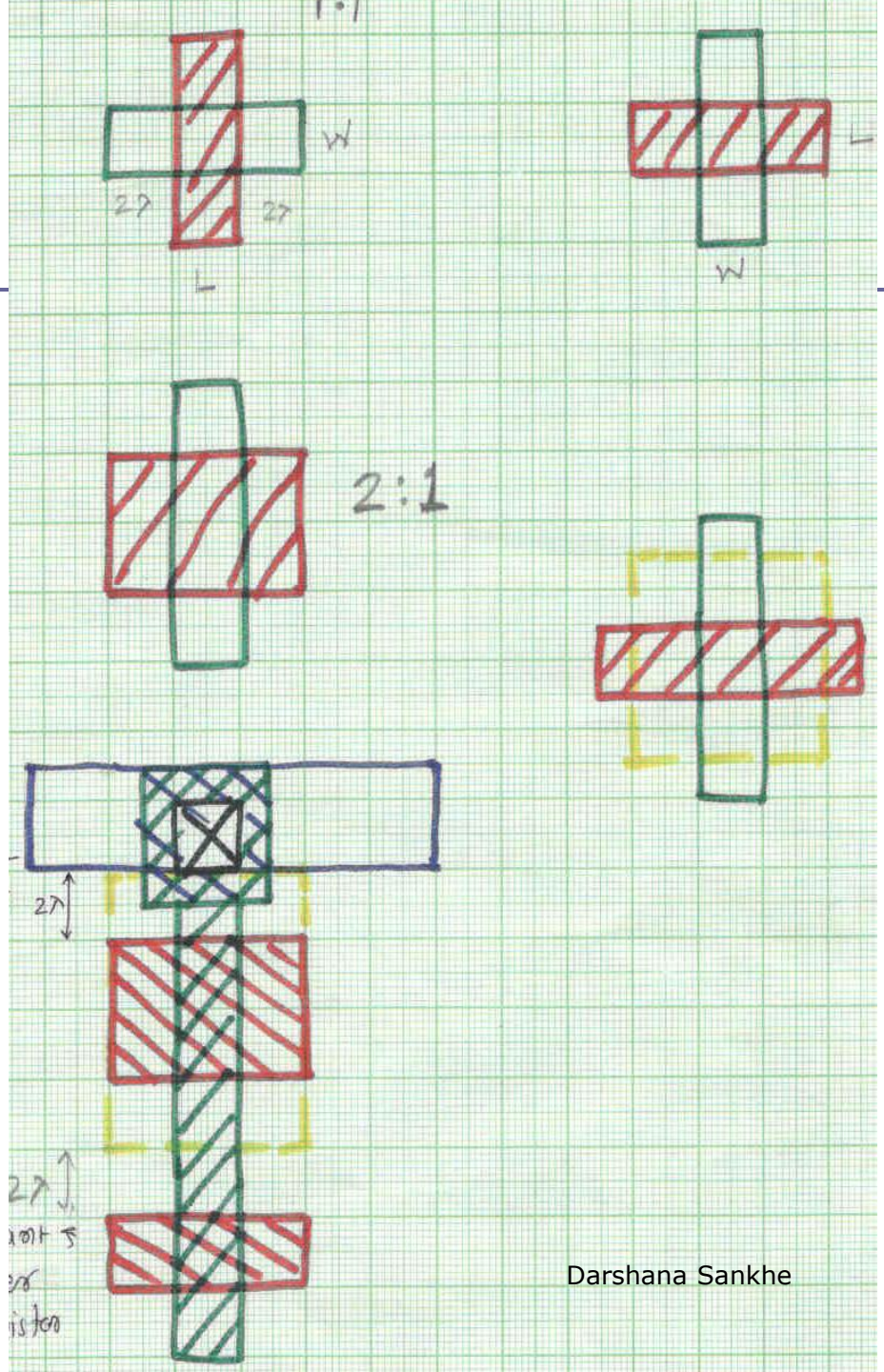
  (depletion regions tend to spread outward)
- metal-metal spacing 3λ

- diff-poly spacing λ

Design Rules: NMOS

- Poly gate extend beyond diff by 2λ

- Diff extend beyond poly by 2λ
- Contact size 2λ * 2λ
- Contact diff/poly/metal overlap 1λ
- Contact to contact spacing 2λ
- Contact to poly/diff spacing 2λ
- Buried contact to active device spacing 2λ
- Buried contact overlap in diff direction 2λ
- Buried contact overlap in poly direction 1λ
- Implant gate overlap 2λ



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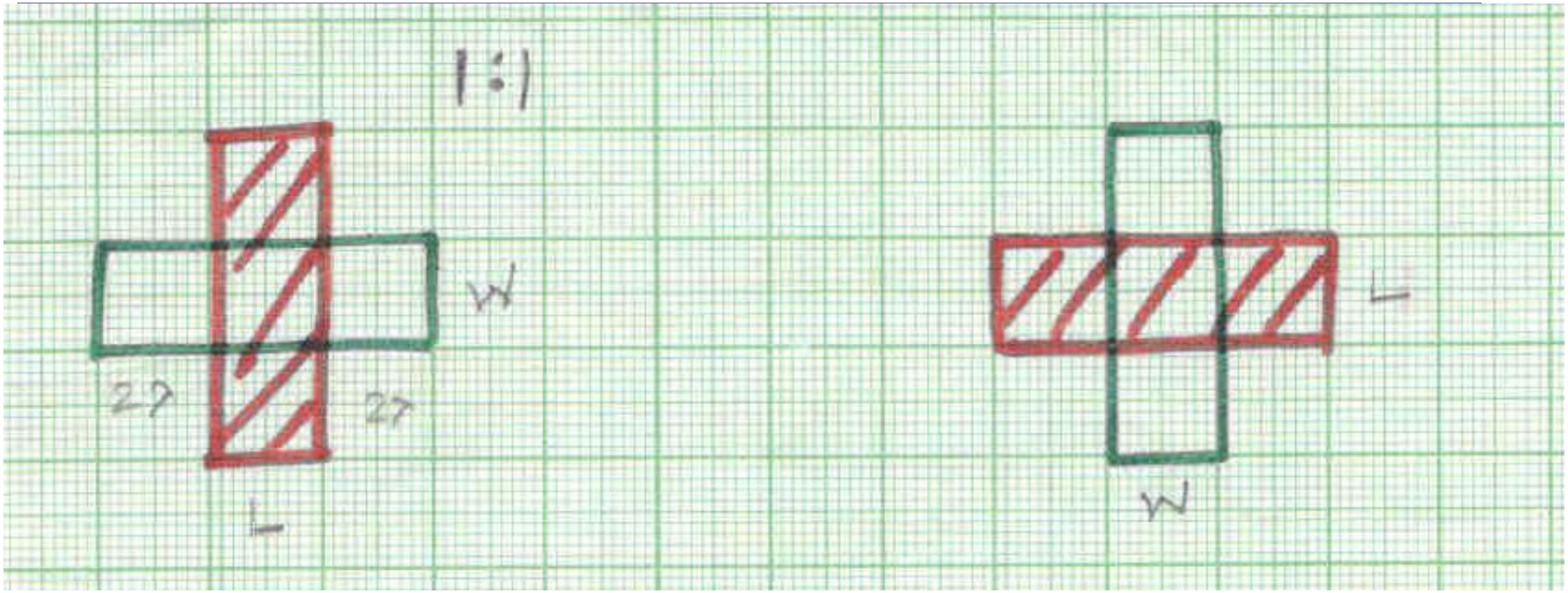

1:1
W
2?
2?
L
L
W

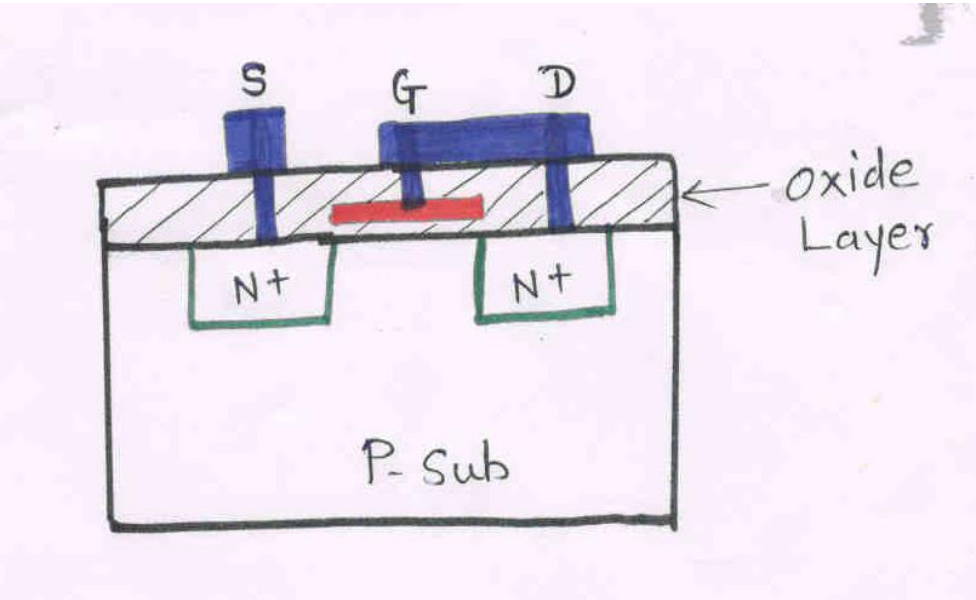
Interlayer Contacts :

- Interconnection between poly and diffusion is done by contacts.

- Metal contact
- Butting contact
- Buried contact

Metal contact :

- Contact cut of 2λ * 2λ in oxide layer above poly and diffusion
- Metal used for interconnection
- Individual contact size becomes 4λ * 4λ



Butting Contact

- The gate and diffusion of NMOS device can be connected by a **butting contact.**

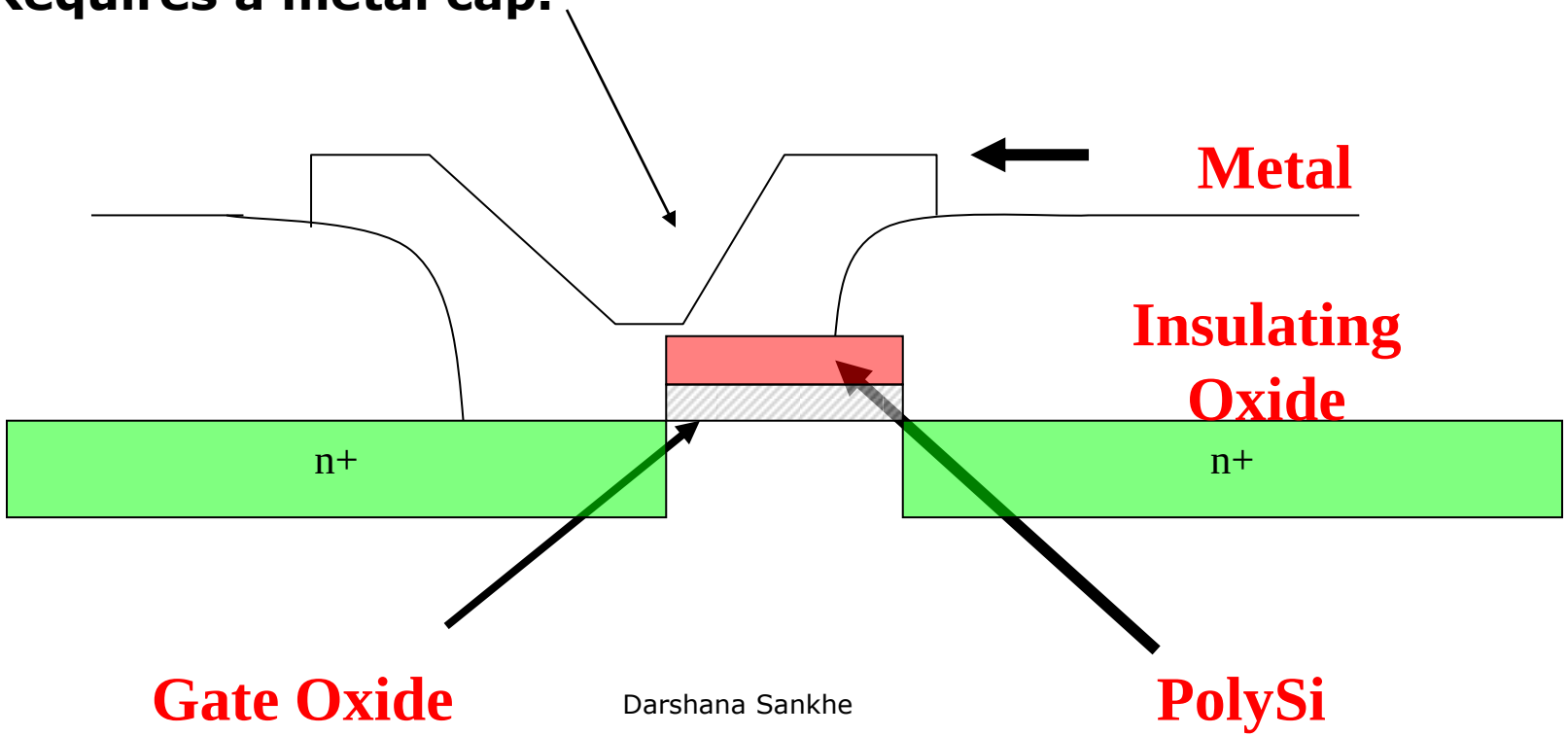
- **Two contact cuts are adjacent to each other**
- **Therefore effective contact area is less**

- Here metal makes contact to both the diffusion forming the drain of the transistor and to the polySi forming this device's gate.

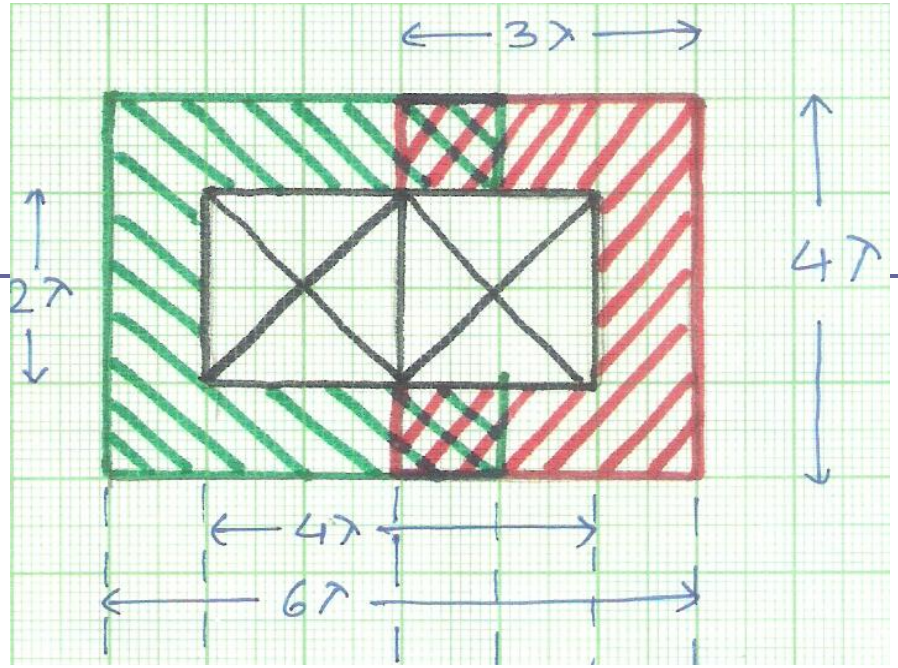
Butting Contact

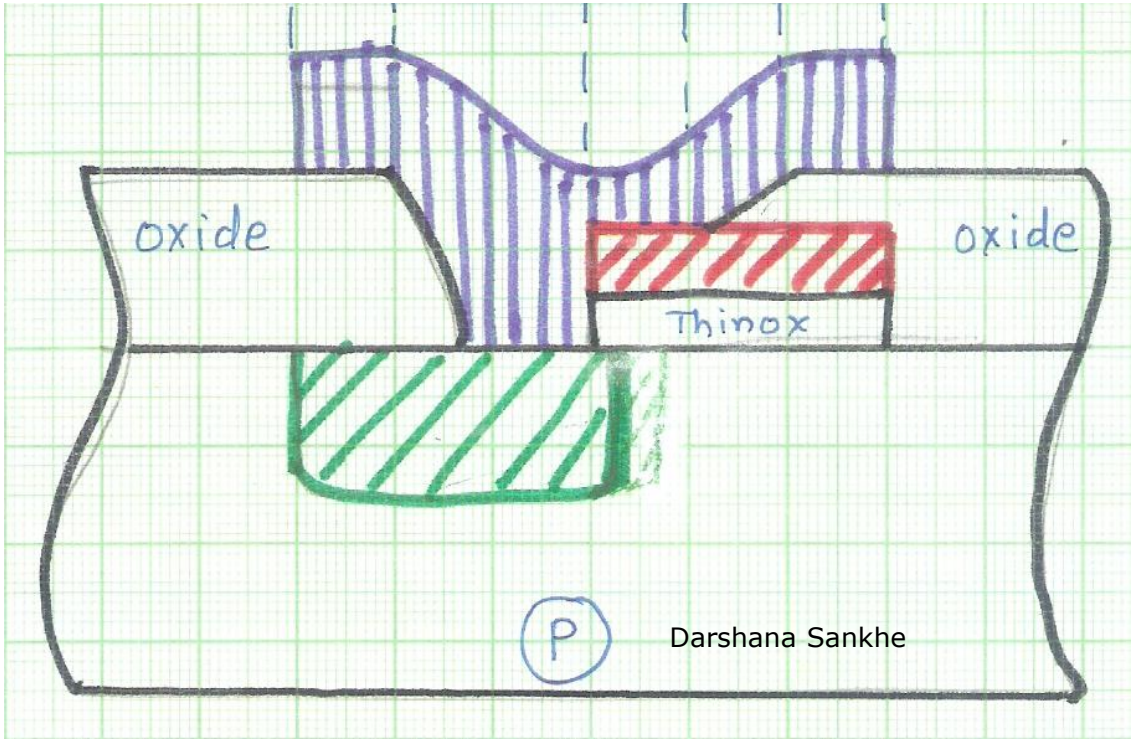
Disadvantages:

- **Metal descending the hole has a tendency to fracture at the polySi corner, causing an open circuit.**
- **Requires a metal cap.**



Butting Contact :





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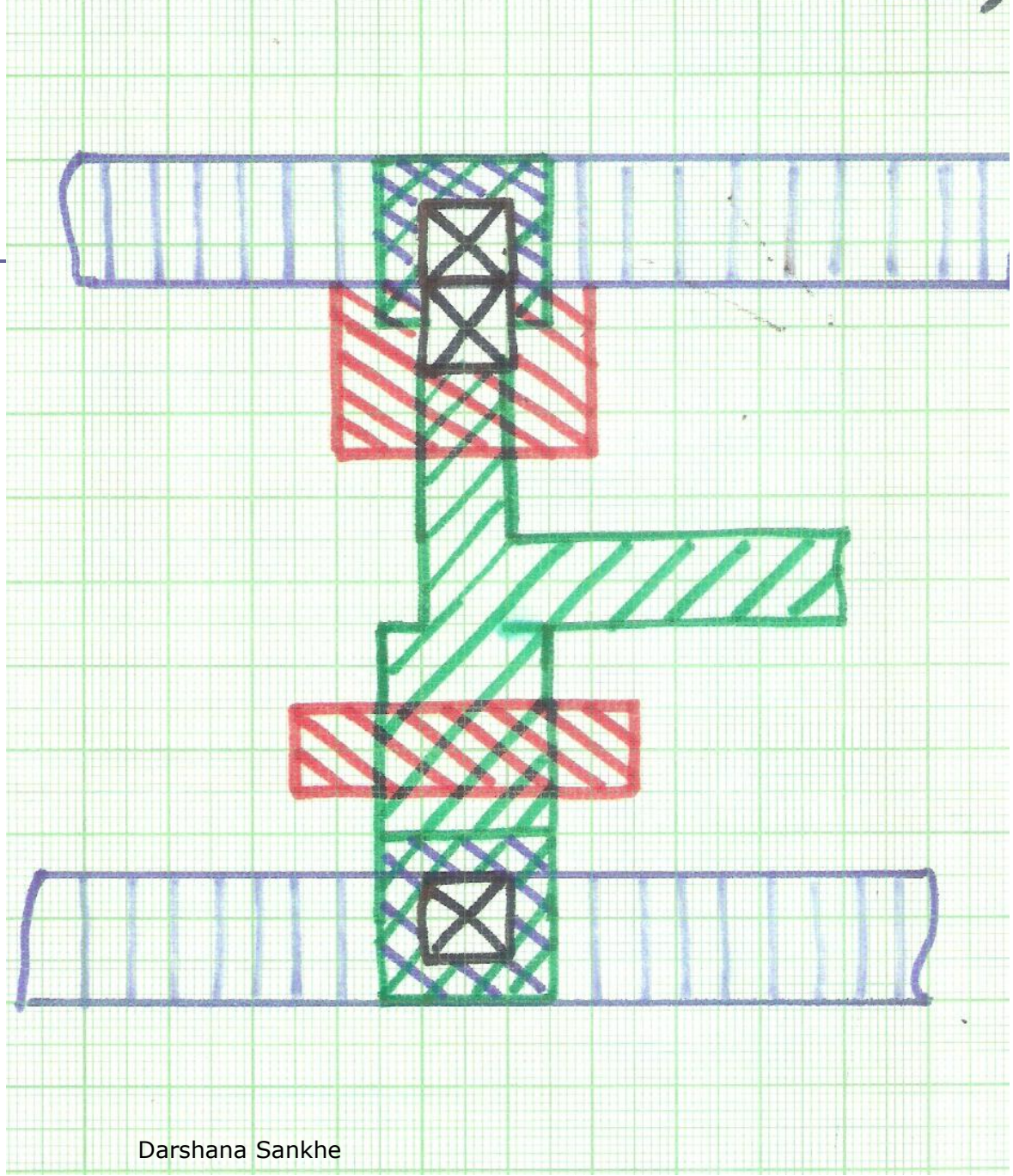
Butting Contact

- Metallization is required only over the butting contact holes which are 2 λ x 4λ in size
- A border of width λ around all four sides is added to allow for mis-registration and to ensure proper contact.
- This brings the metallization size to 4λ x6λ

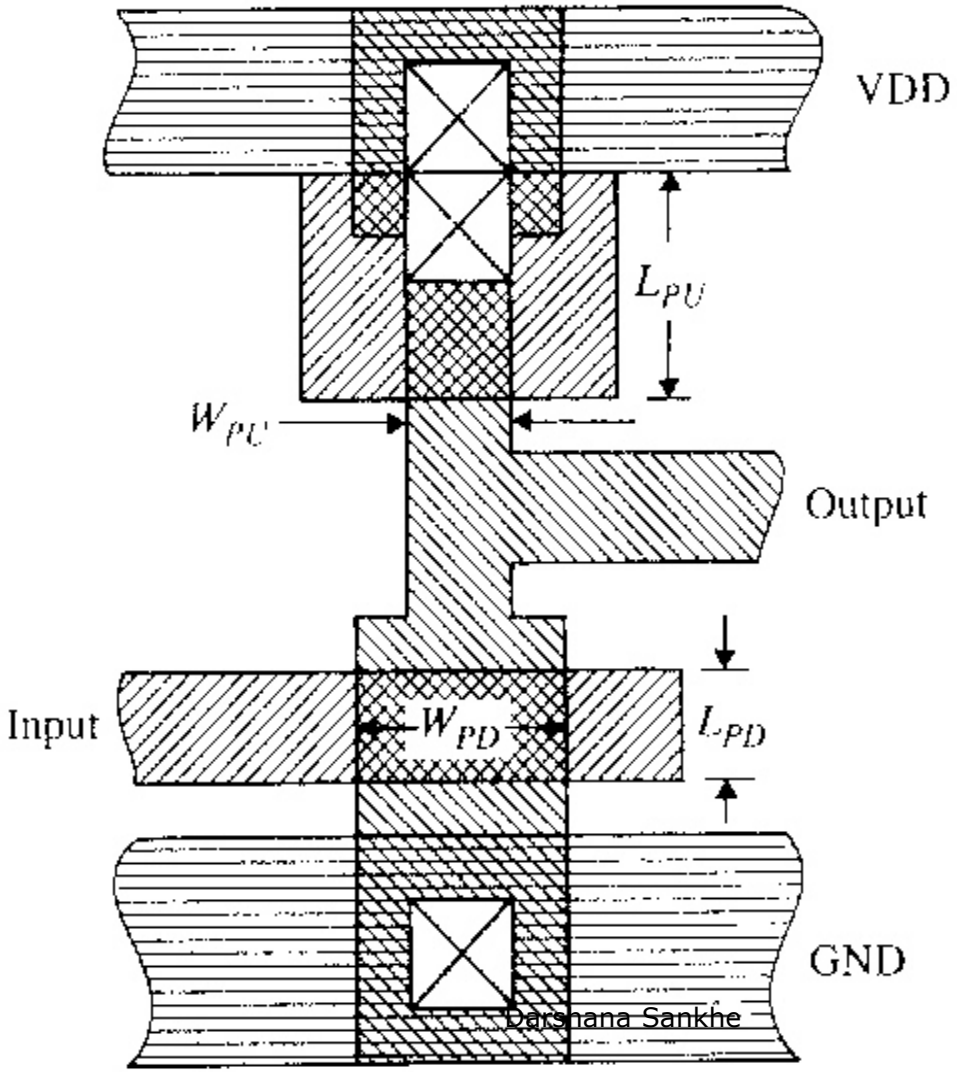
Advantage:

- No buried contact mask required and avoids associated processing.

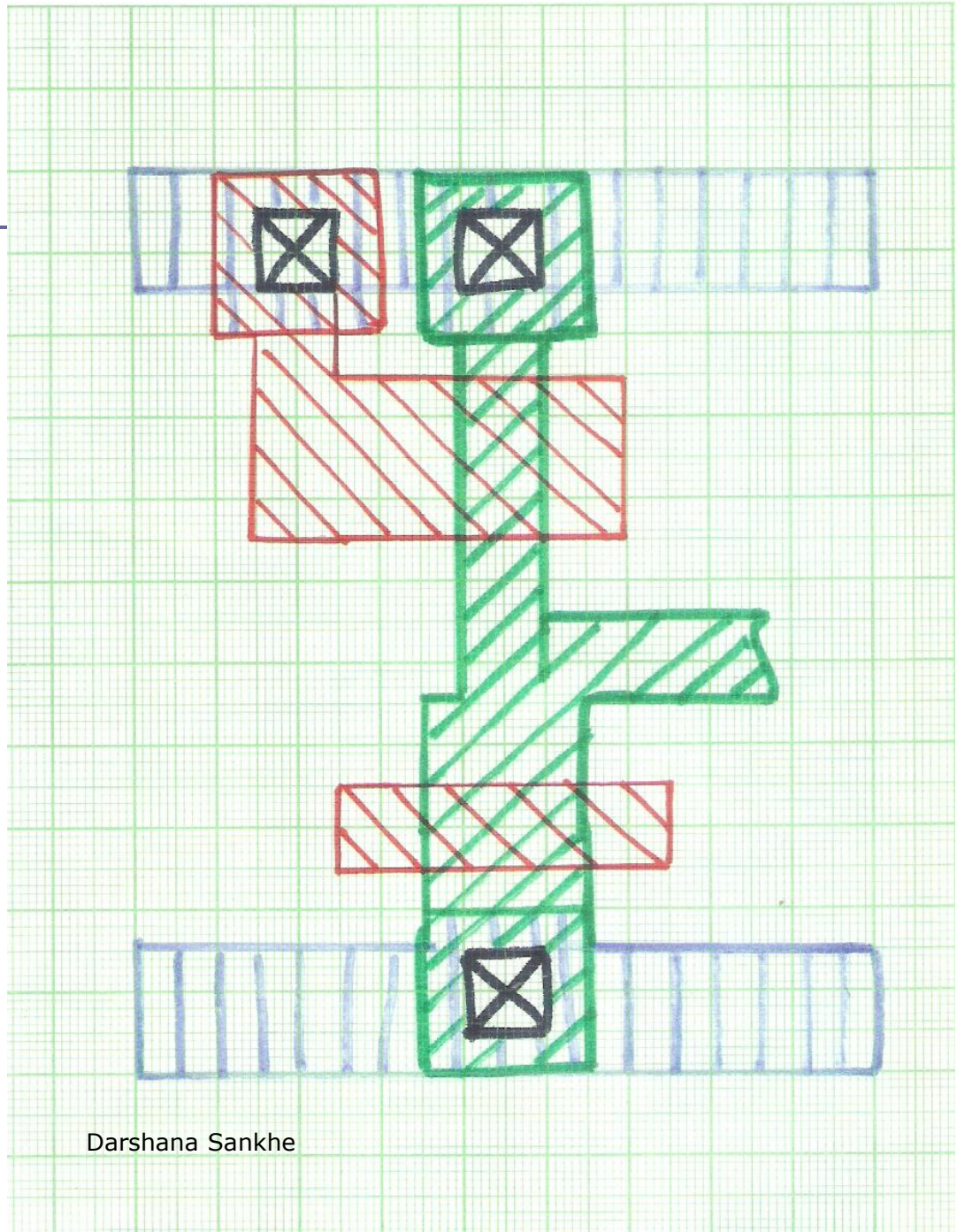
NMOS INVERTER- Enhancement load



NMOS INVERTER: Enhancement Load



NMOS INVERTER- Enhancement load



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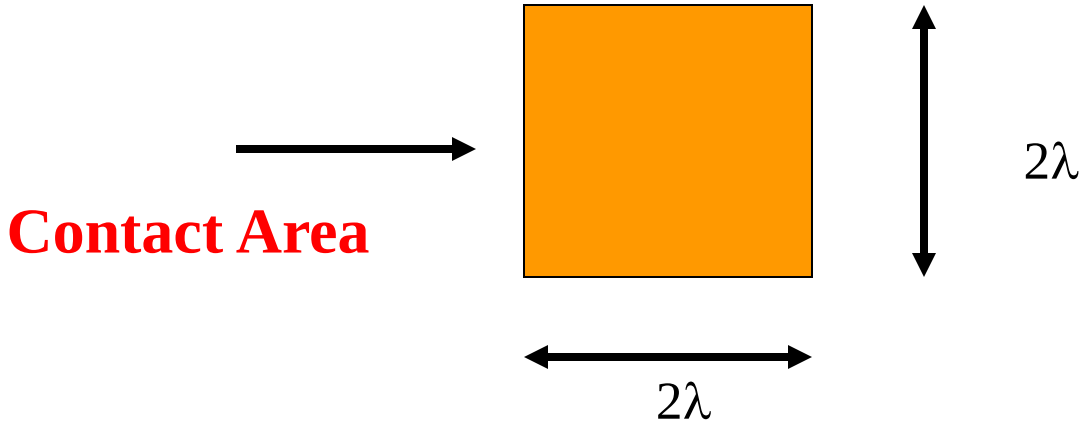
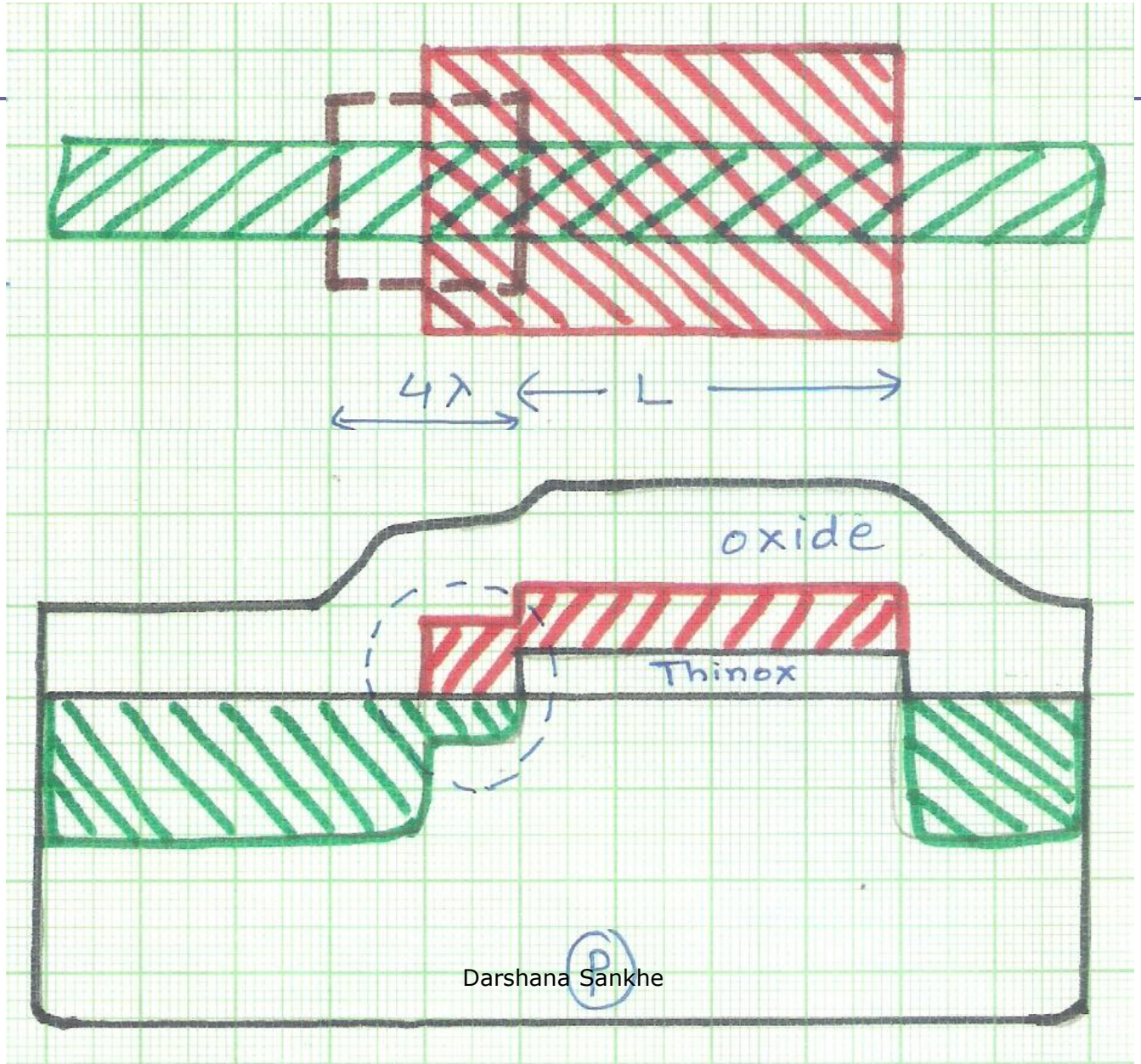
Buried Contact

- The buried contact window defines the area where oxide is to be removed so that polySi connects directly to diffusion.
- Contact Area must be a min. of 2 λ *2λ to ensure adequate contact area.

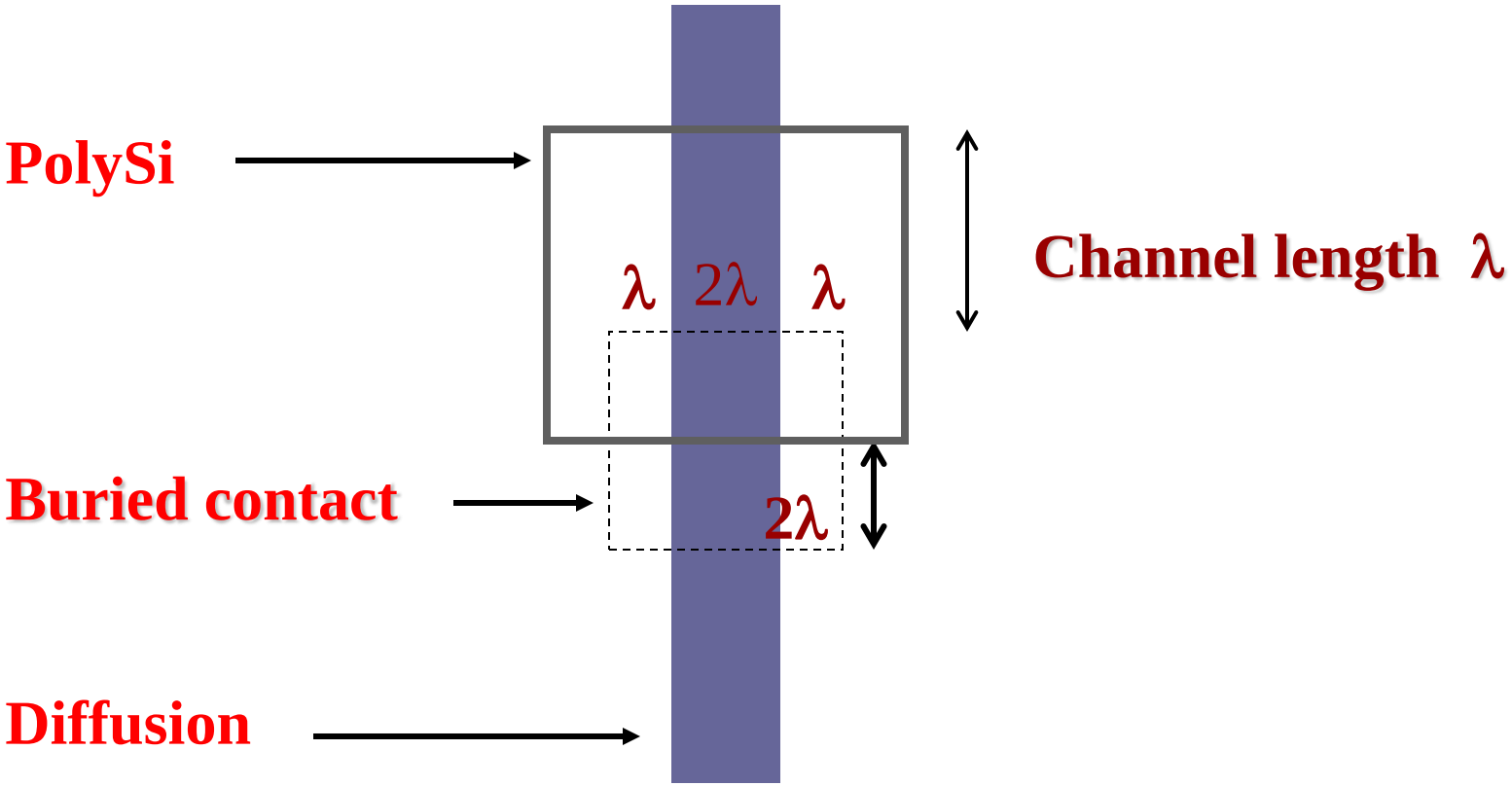


- Advantages: No metal cap required.
- Disadvantage: An extra mask is required.

Buried contact :



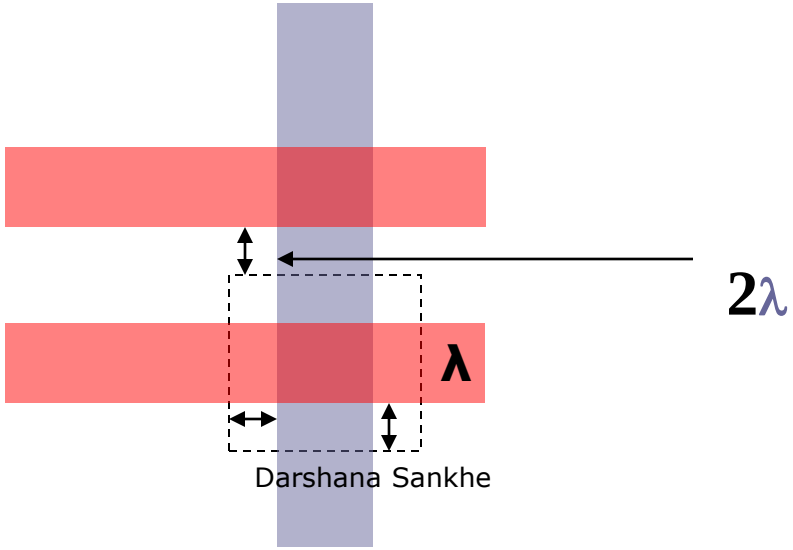
Buried Contact

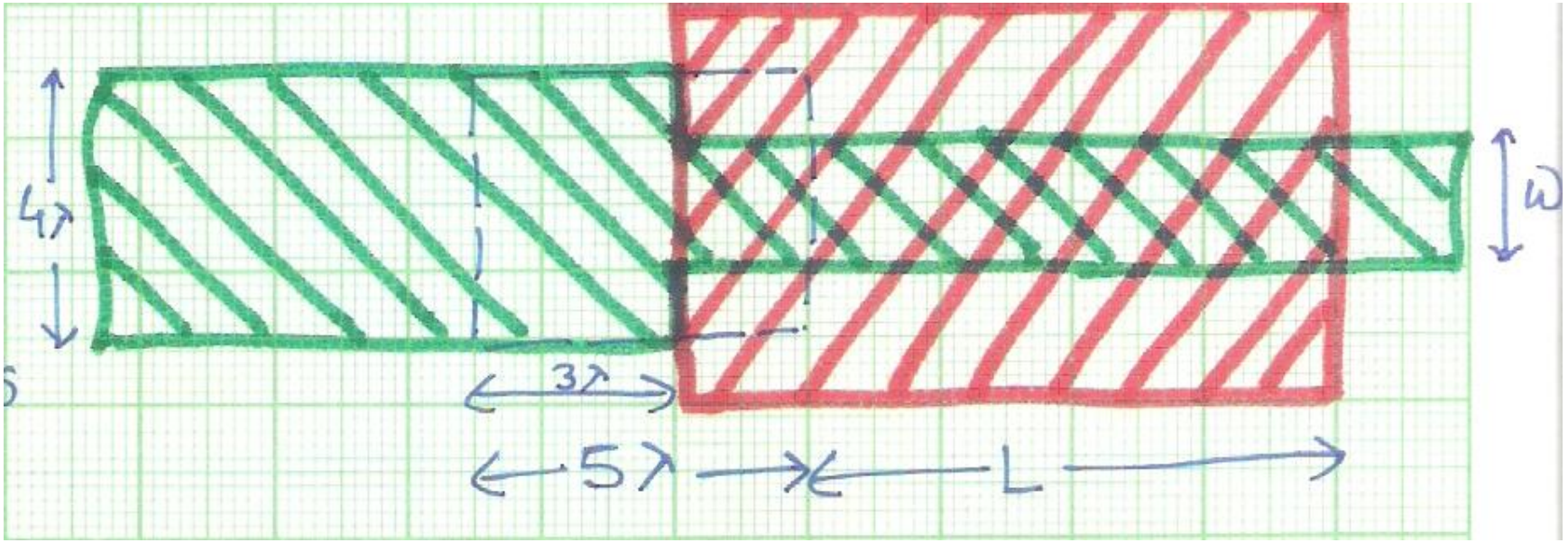


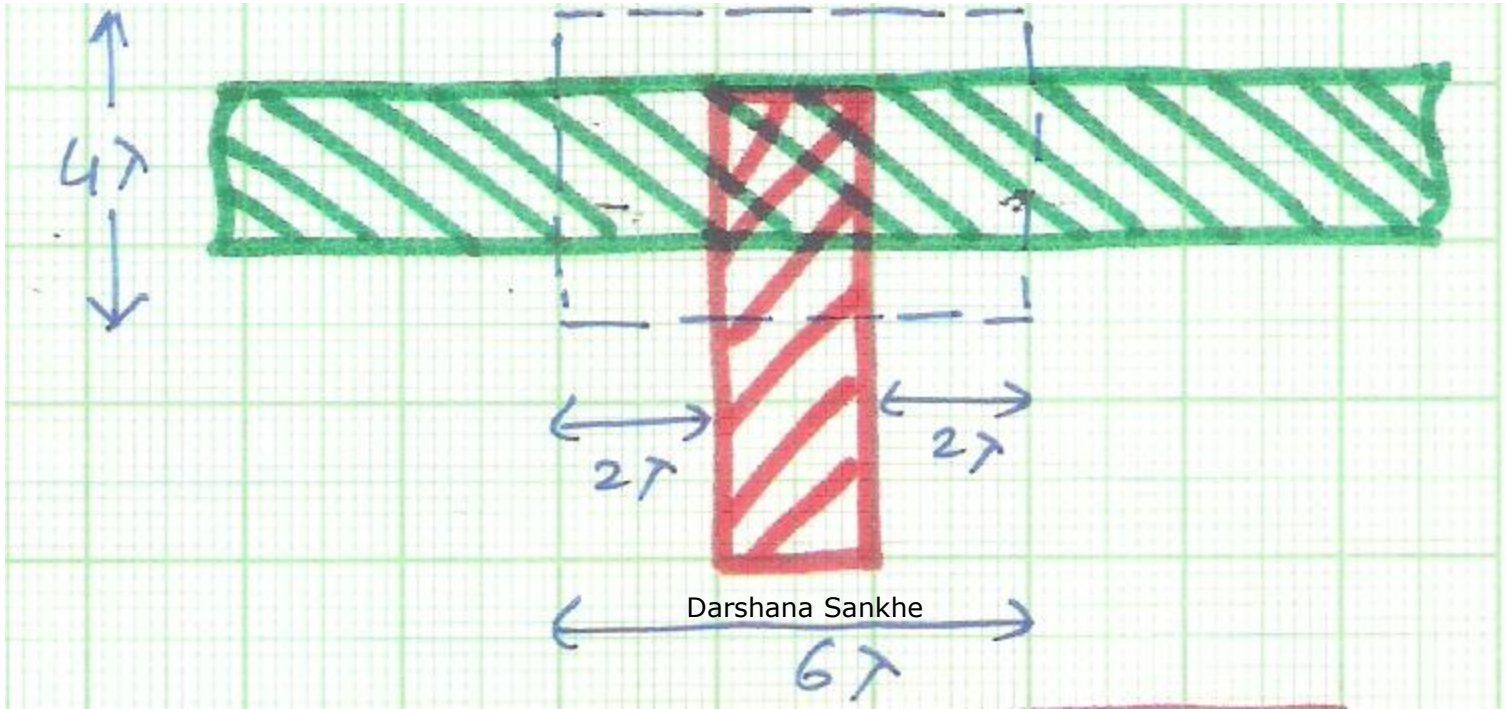
Buried Contact

- The buried contact window surrounds this contact by λ in all directions to avoid any part of this area forming a transistor.

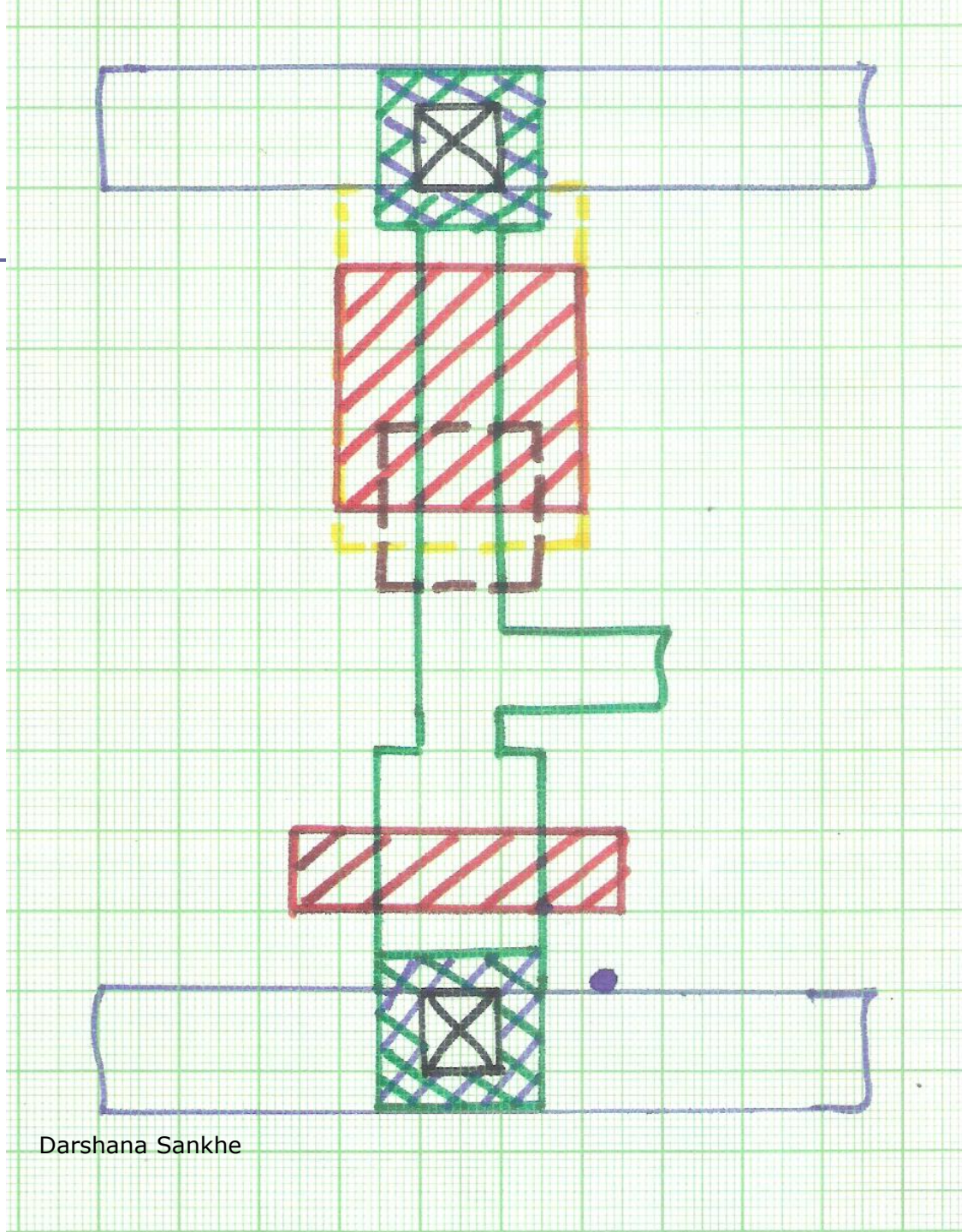
- Separated from its related transistor gate by 2λ to prevent gate area from being reduced.







NMOS INVERTER
Depletion load



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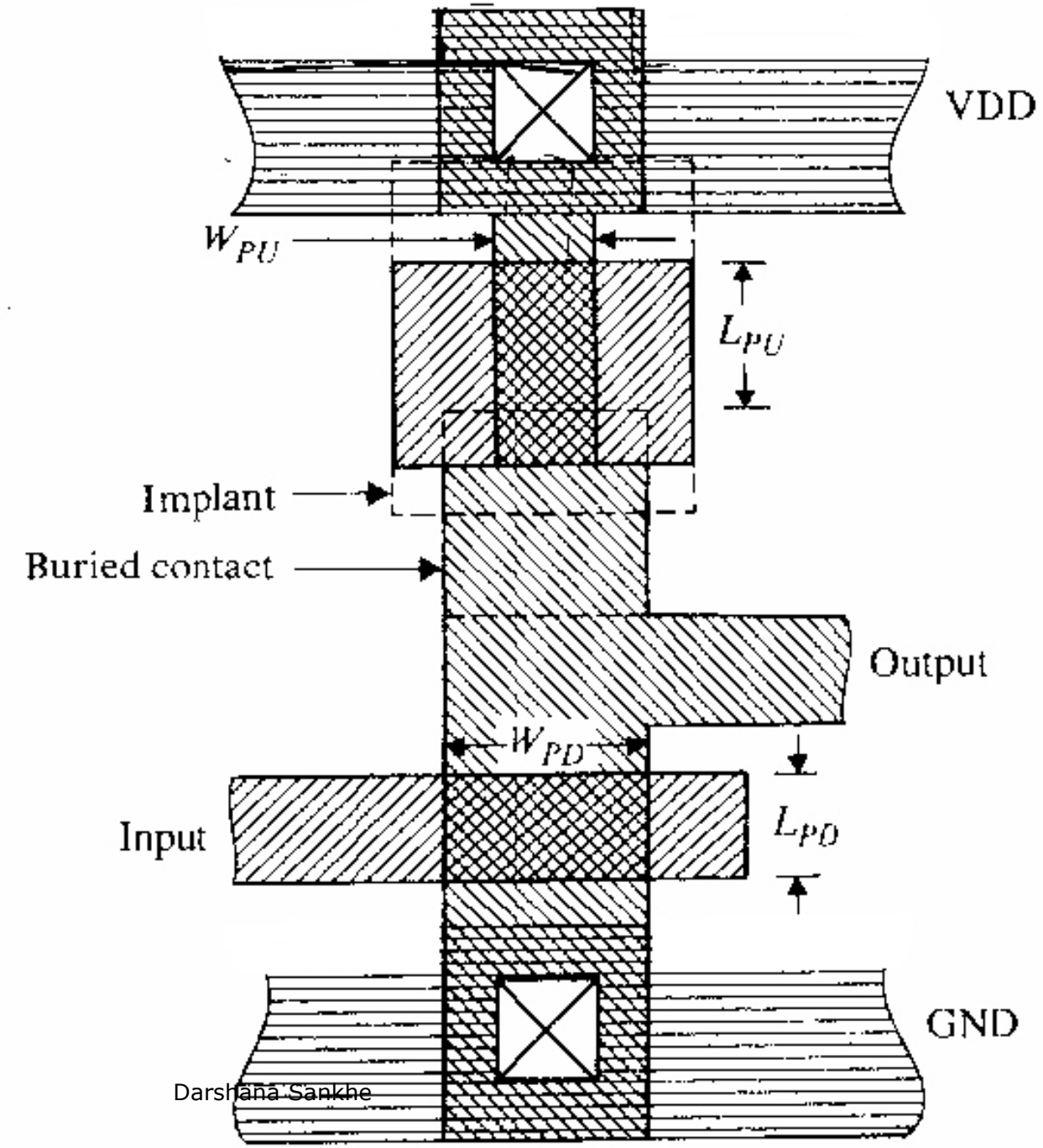
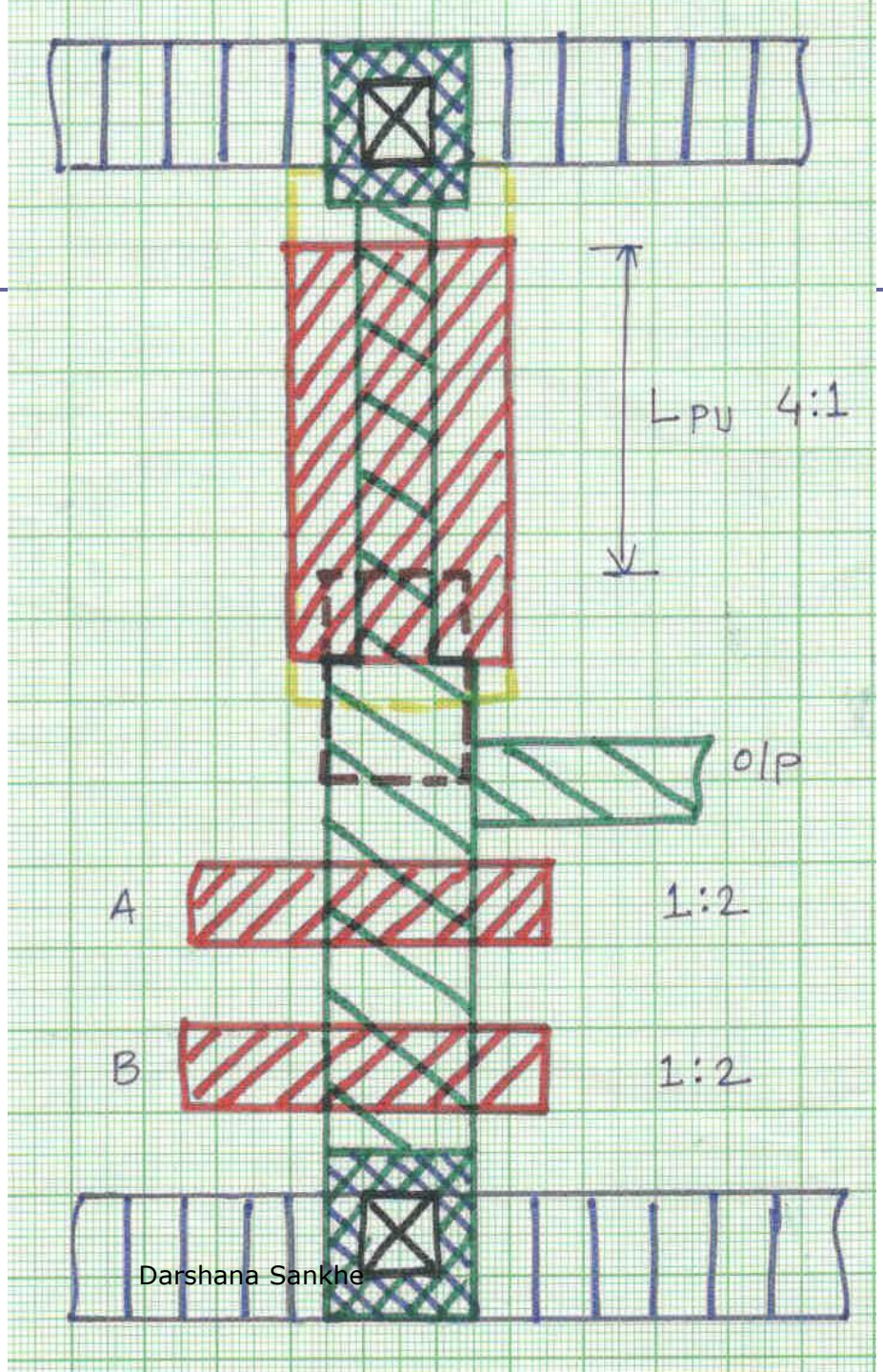
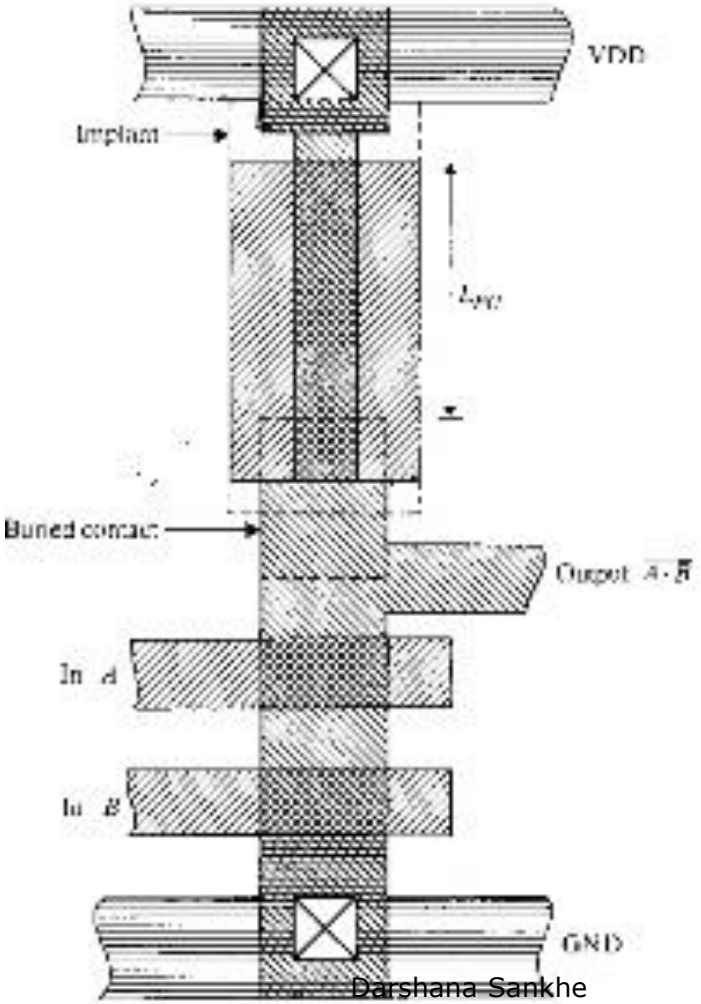
NMOS INVERTER
Depletion Load



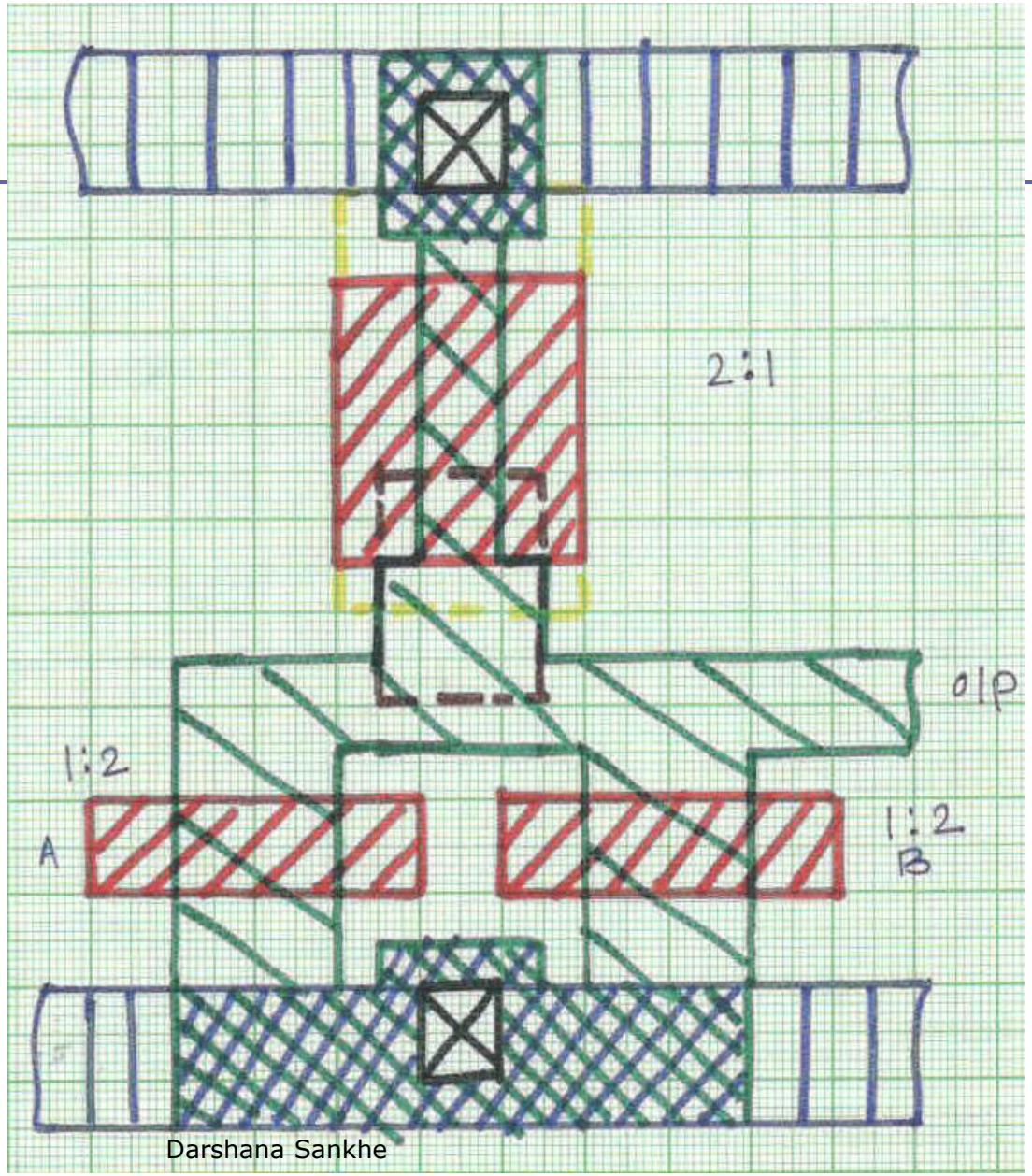
NMOS NAND



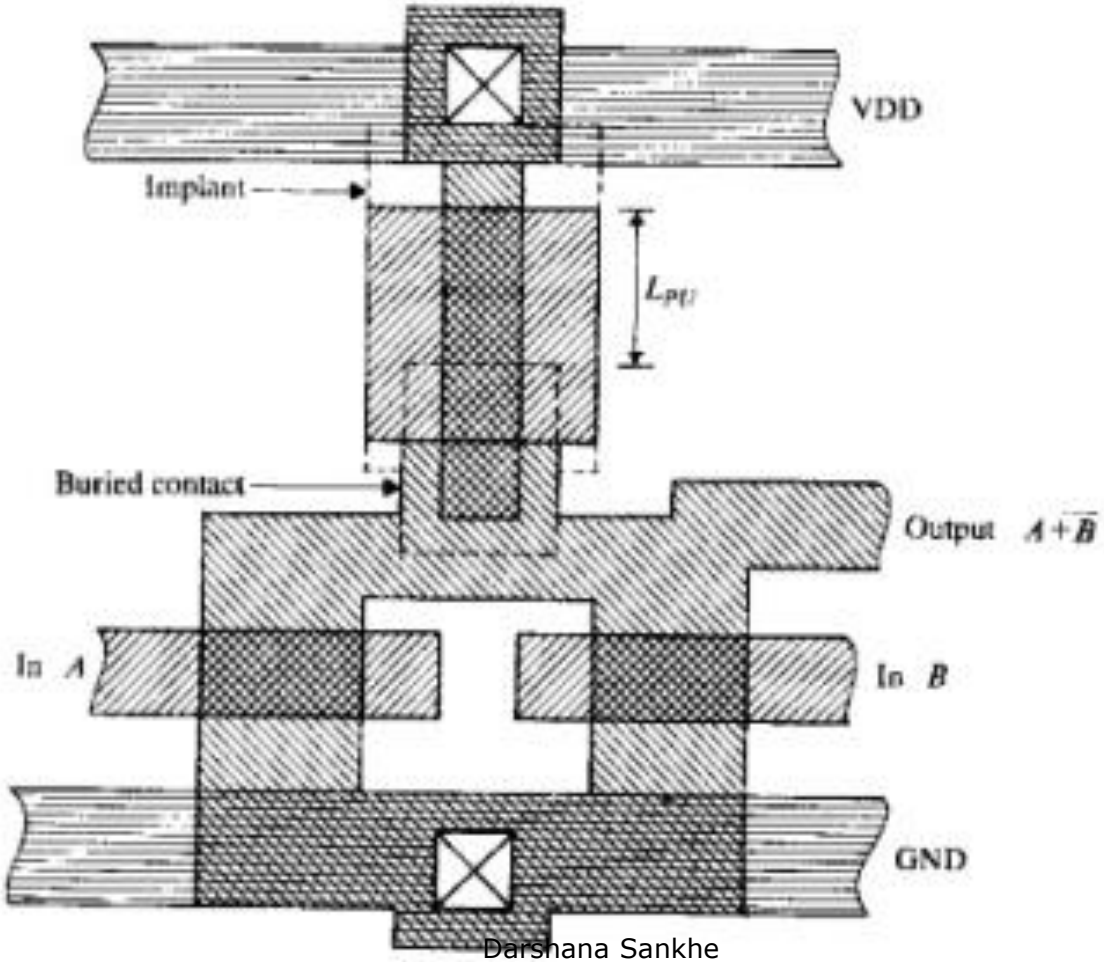
NMOS NAND


VDD
Implant
Buried contact
Output $\overline{A \cdot B}$
In A
In B
GND

NMOS NOR



NMOS NOR: Layout



(c)

CMOS :

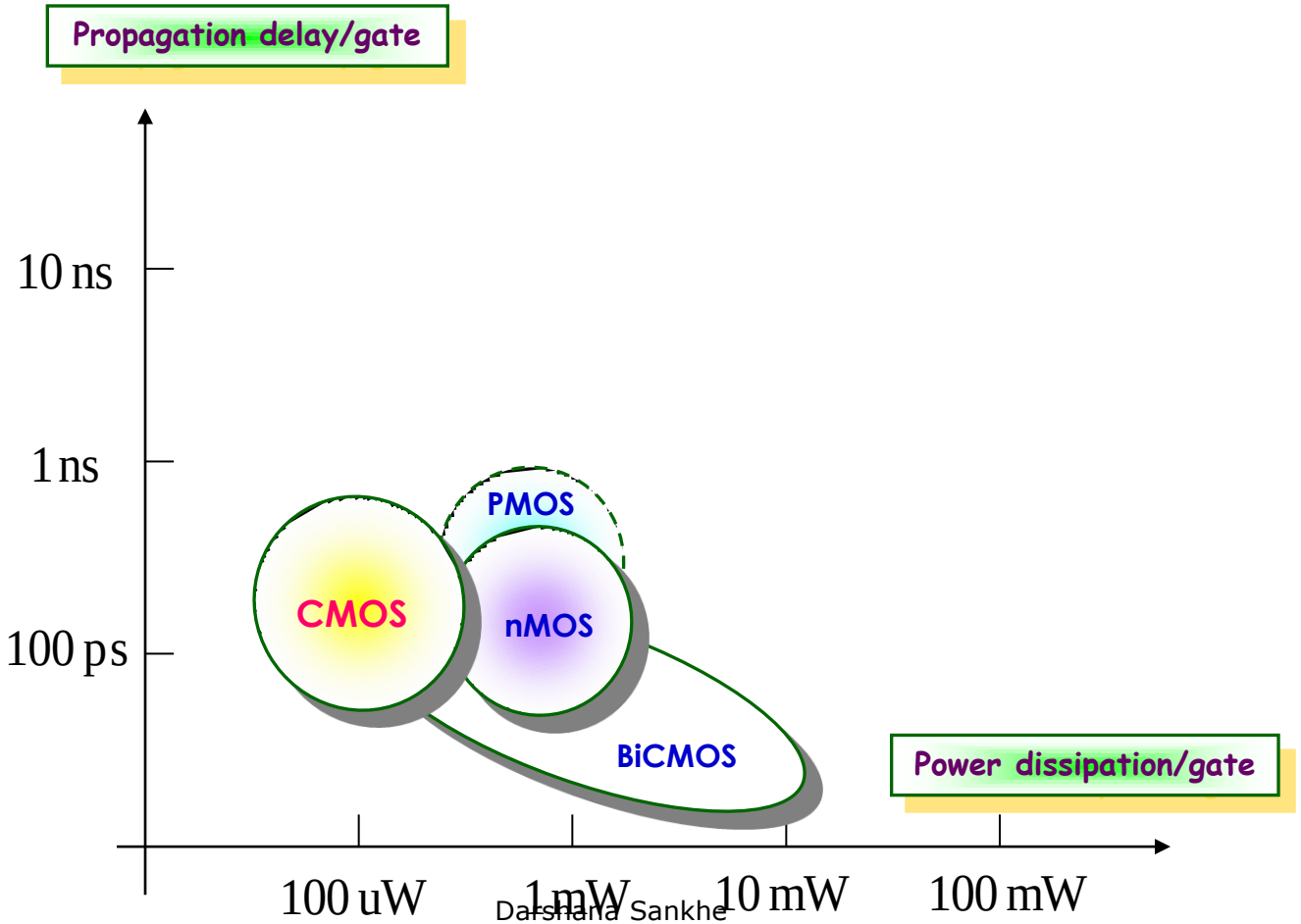
- Pull-up is PMOS
- Pull-down is NMOS

- The channel mobility of electrons is approximately twice of that of holes.

- Conductivity of NMOS is twice, that of identical PMOS.

- But in case of CMOS inverters, one of the devices is always switched off and has very high impedance.

- The noise margin of CMOS circuits is larger than those of NMOS gate operating between same supply rails.


Propagation delay/gate
10 ns
1 ns
100 ps
CMOS
PMOS
nMOS
BiCMOS
Power dissipation/gate
100 uW
1 mW
10 mW
100 mW

Aspect Ratio :

For CMOS:

- R_{inv} = 1:1(Ratioless)
  - As one of the device is always off.
  - 1:1 inverter ratio gives more symmetric layout

Stick Diagram (CMOS): Basic Steps

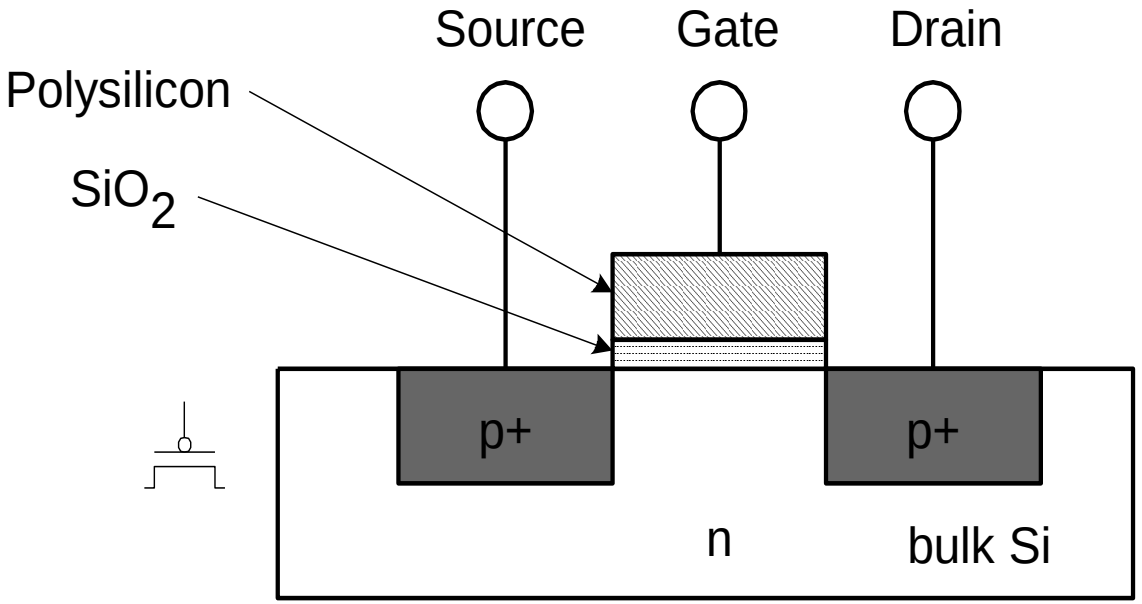
- Steps for CMOS are similar to NMOS
- But one difference is that depletion mode FETs are not used.
- Here, yellow/ brown is used to identify PMOS.
- The two types of FET, n and p, are separated in the diagram by the demarcation line.
- This line represents the well (n/p-well).
- Above this line are all p-type MOSFETs.
- Below this line n-type MOSFET are present.

Stick Diagram (CMOS): Basic Steps

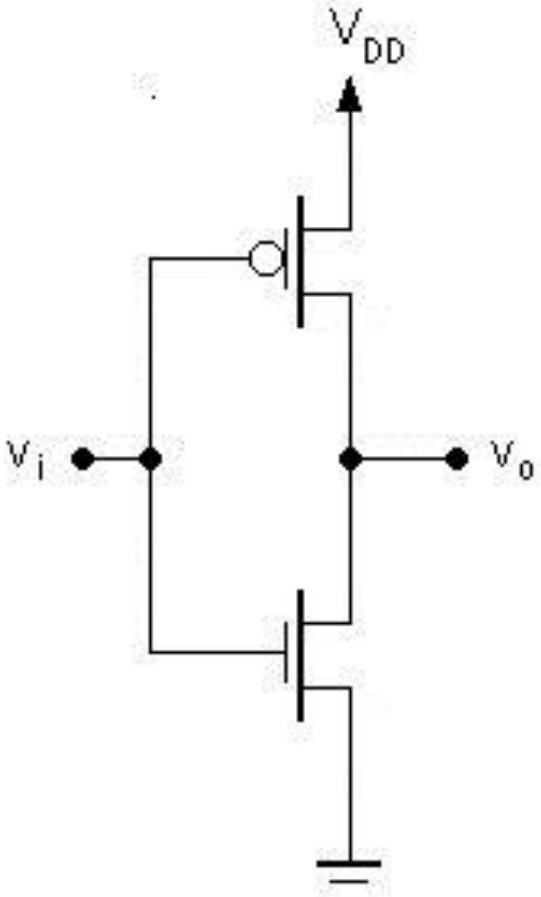
- No Diffusion can cross demarcation line.
- Only poly and metal can cross demarcation line
- N-diffusion and p-diffusion are joined using a metal wire.
- First step is to draw two parallel rails for VDD and GND.
- Next draw a demarcation line (brown)
- Place all PMOS above and NMOS below this line.
- Connect them using wires (metal).

PMOS :

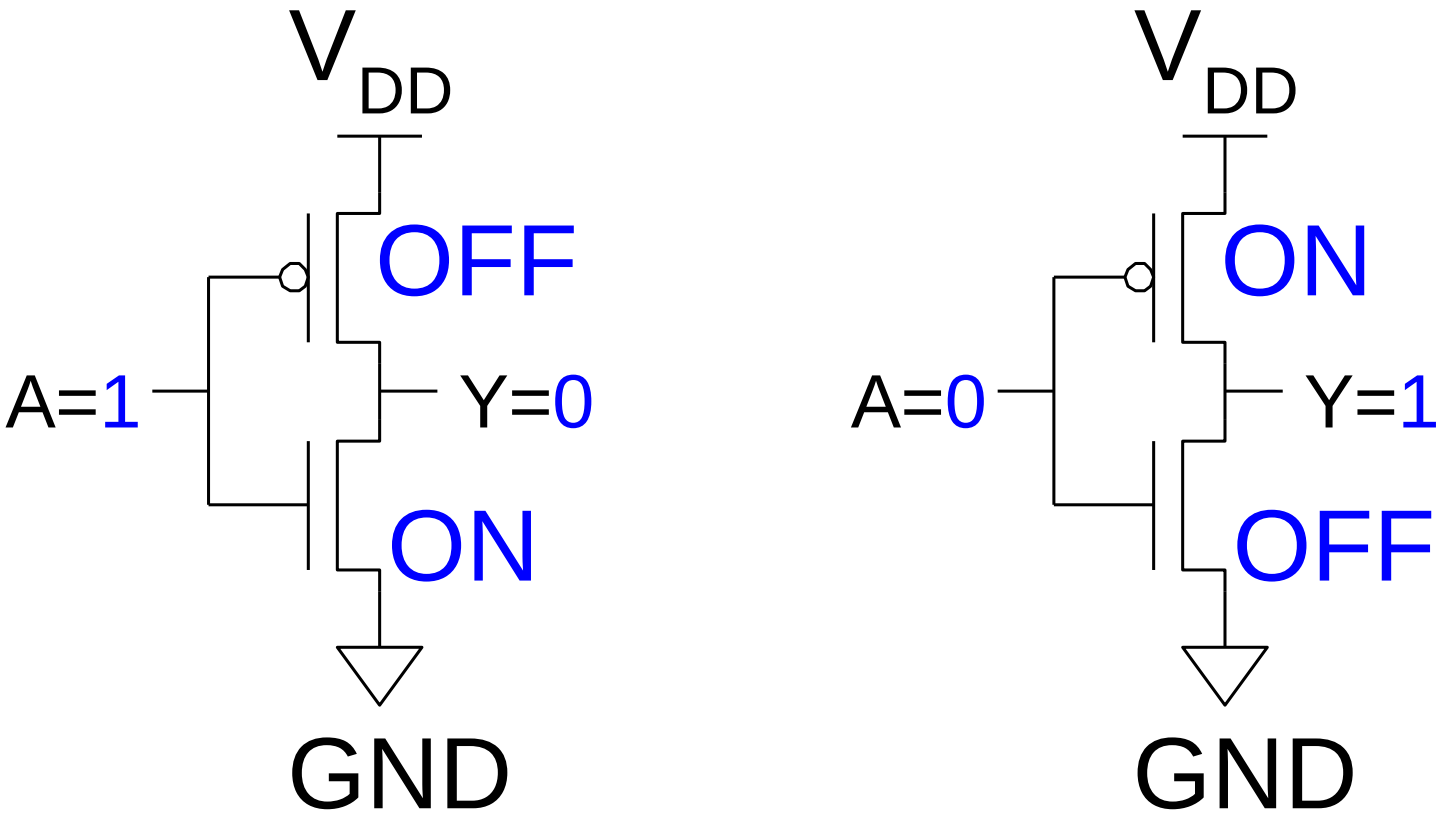
- Body tied to high voltage (V_{DD})
- Gate low: transistor ON
- Gate high: transistor OFF
- Bubble indicates inverted behavior



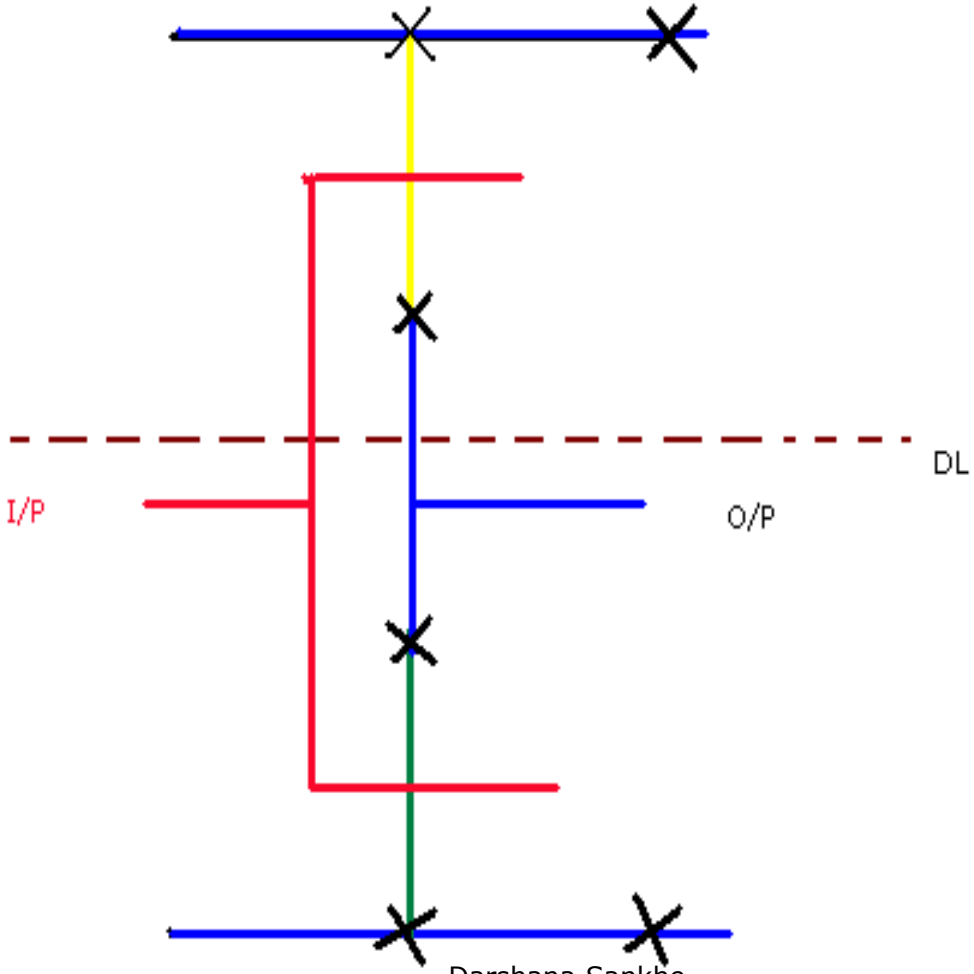
CMOS Invertor (Cicuit Diagram)



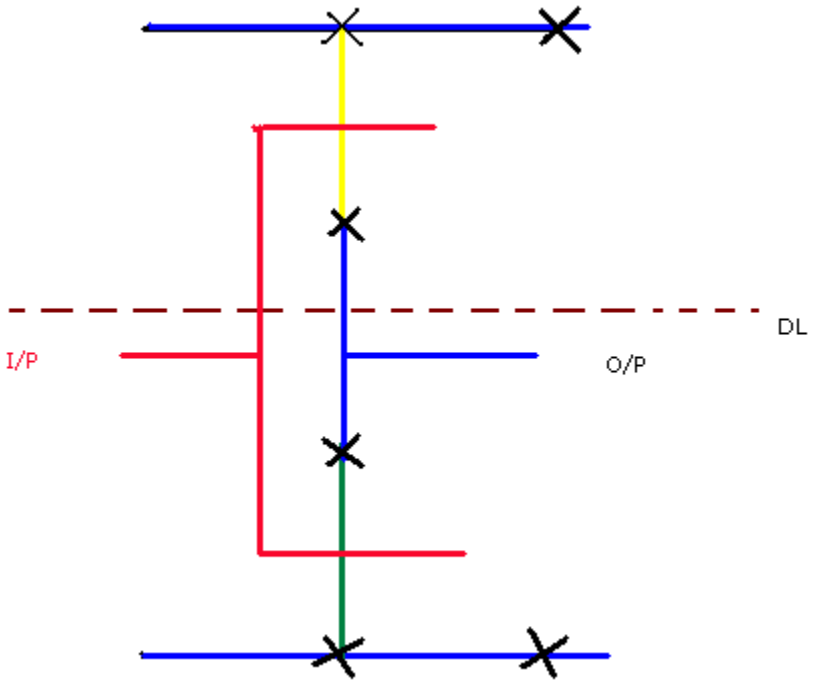
CMOS Inverter :

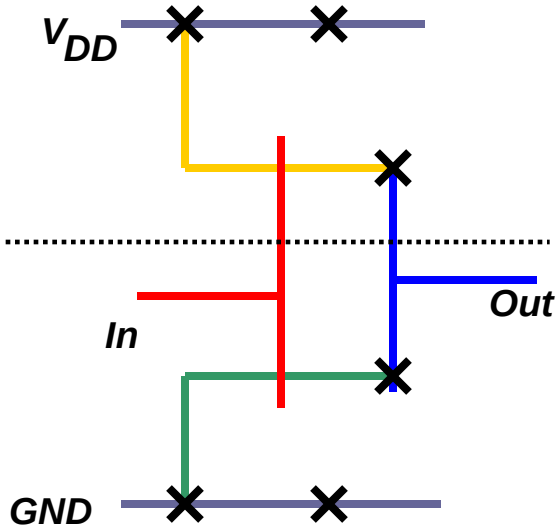


CMOS Invertor (Stick Diagram)



CMOS Invertor (Stick Diagram)

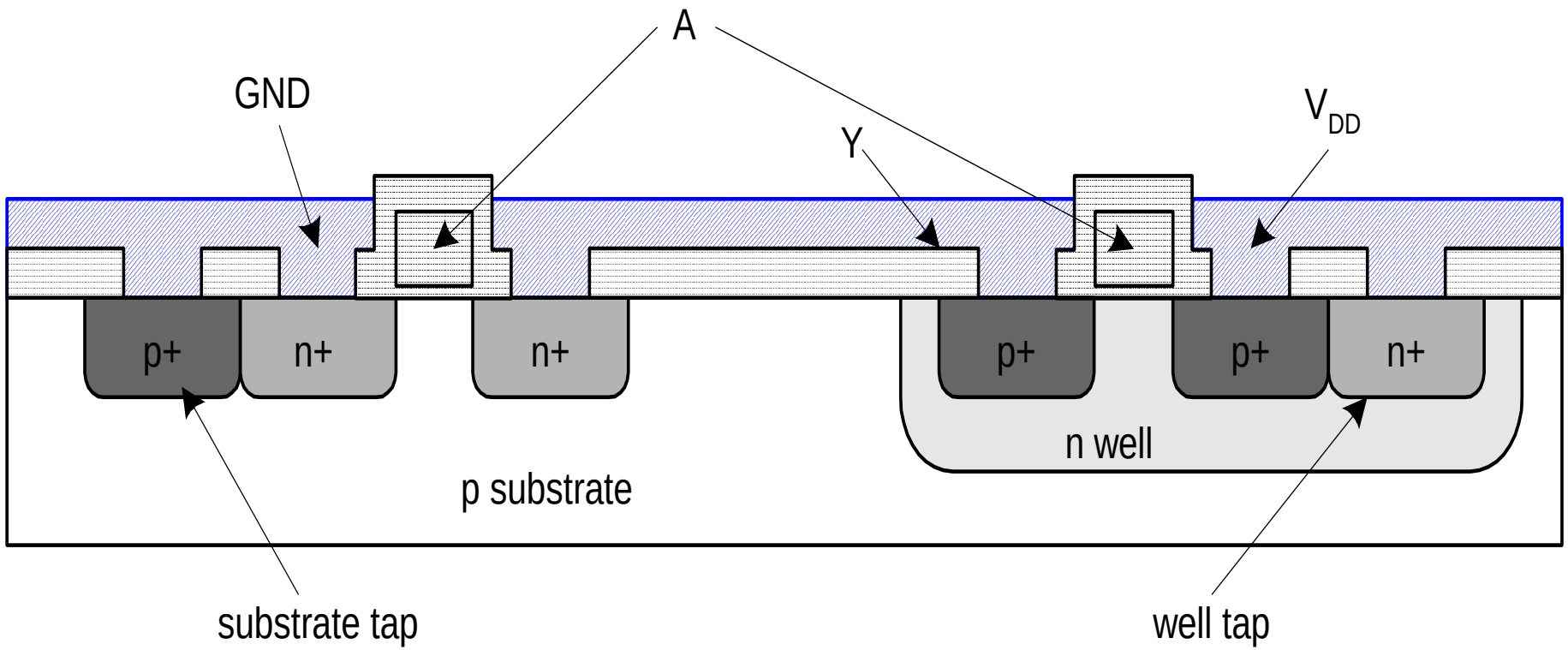




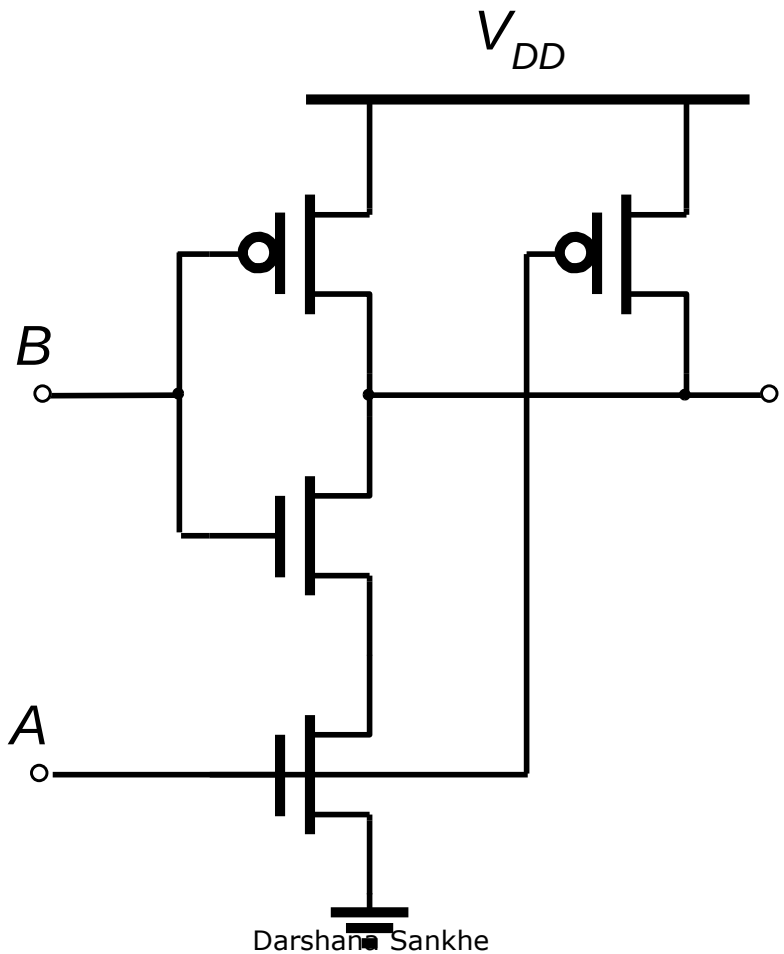
Well Biasing :

- The various N and P diffusions must be reverse biased to ensure that those wells are insulated from each other.
- This requires that the N- wells are connected to the most positive voltage, VDD.
- The P- substrate must be connected to the most negative voltage, ground.
- This assumes that all other nets are at a voltage between 0V and VDD.

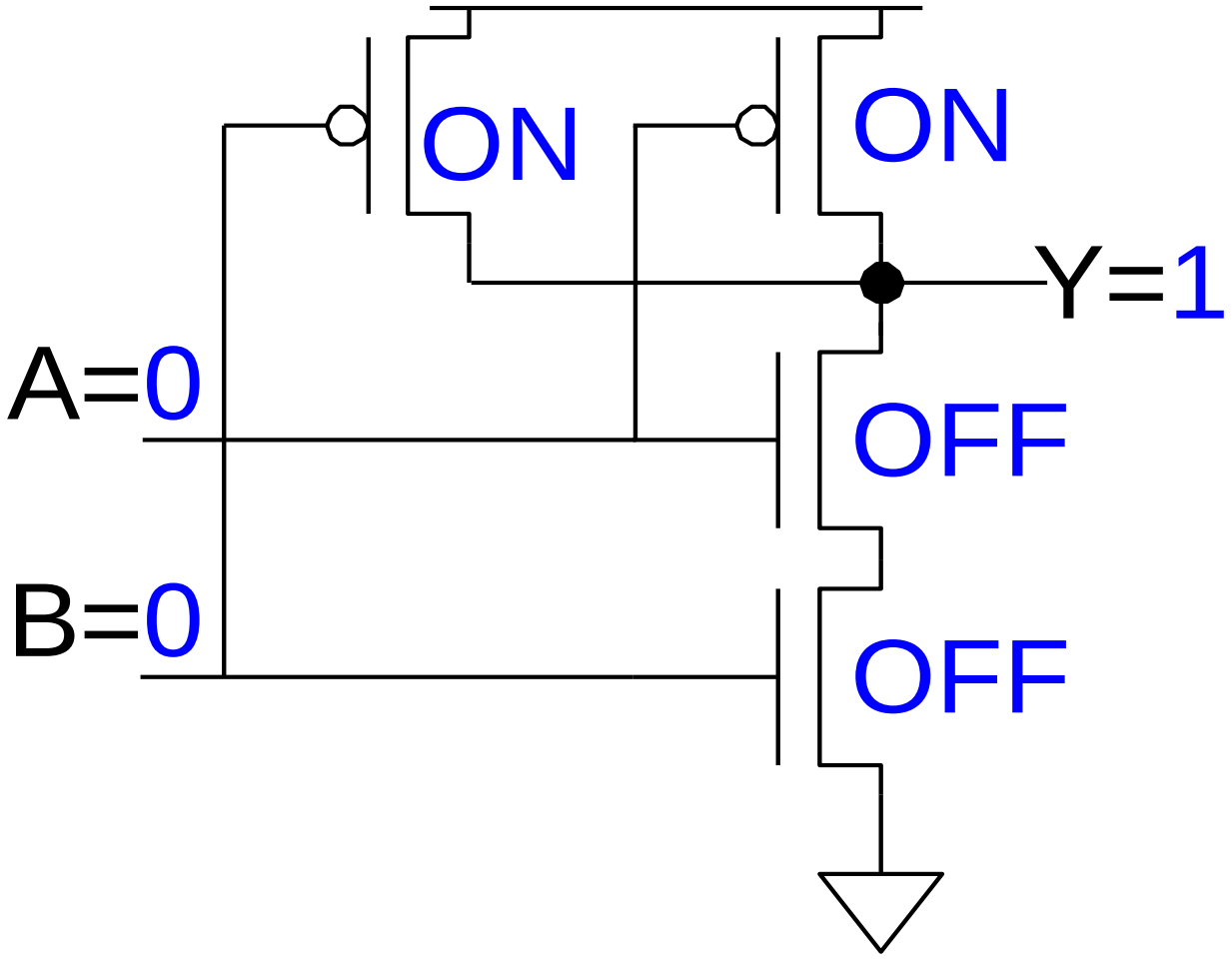
CMOS INVERTER :

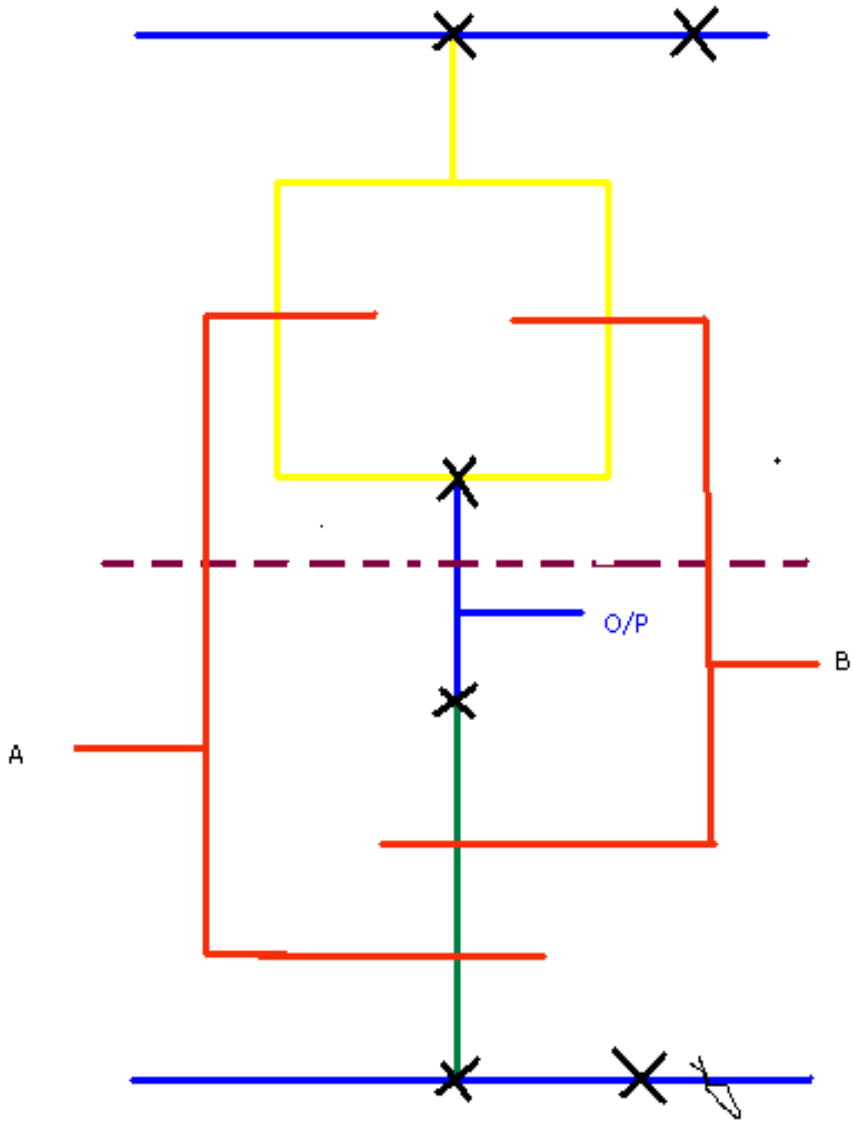


CMOS NAND (Cicuit Diagram)



CMOS NAND:





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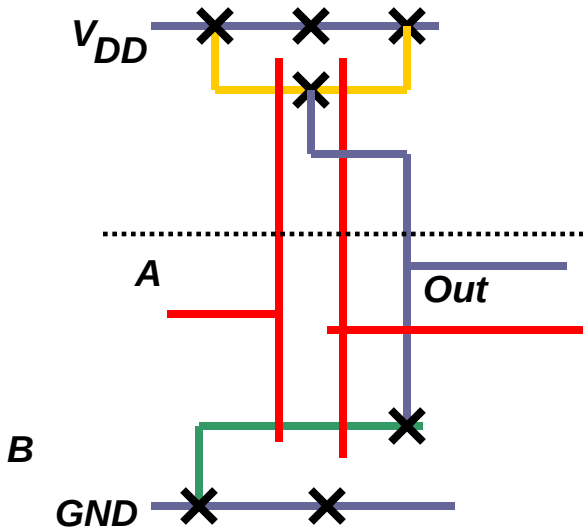
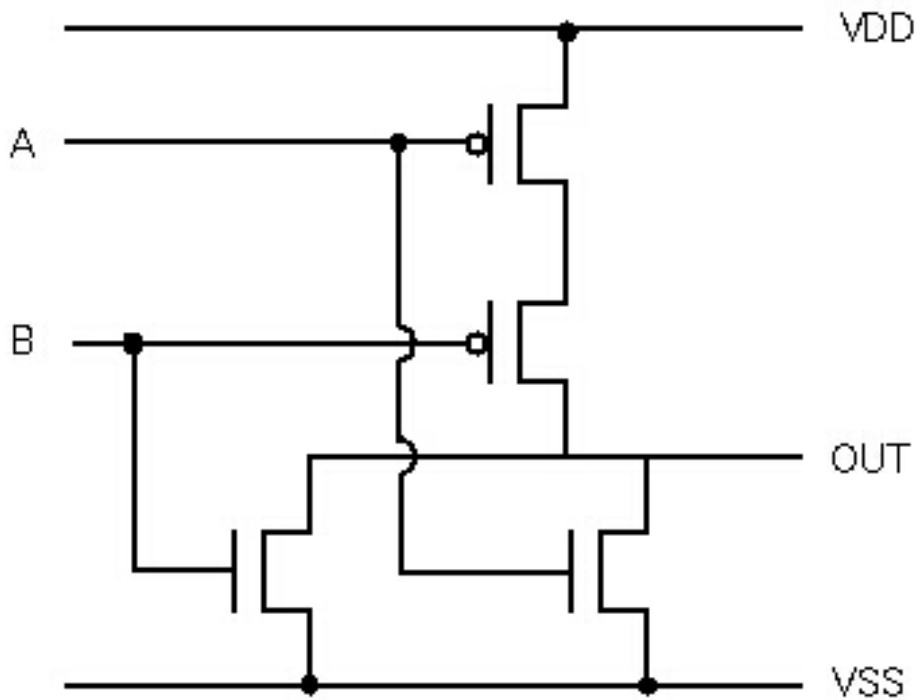
CMOS NAND (Stick Diagram)

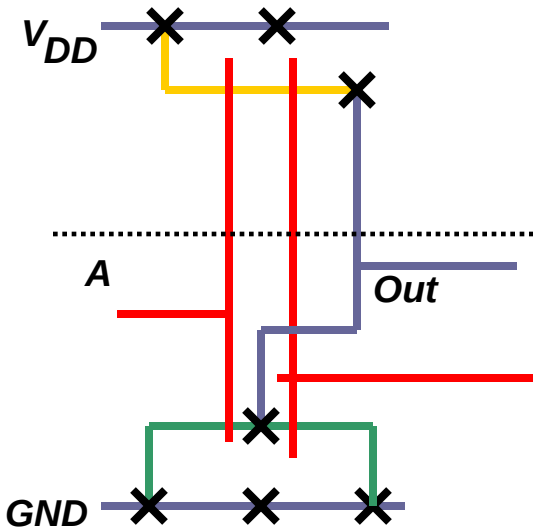


CMOS NOR (Cicuit Diagram)



NOR gate in CMOS

CMOS NOR (Stick Diagram)



Design Rules: CMOS

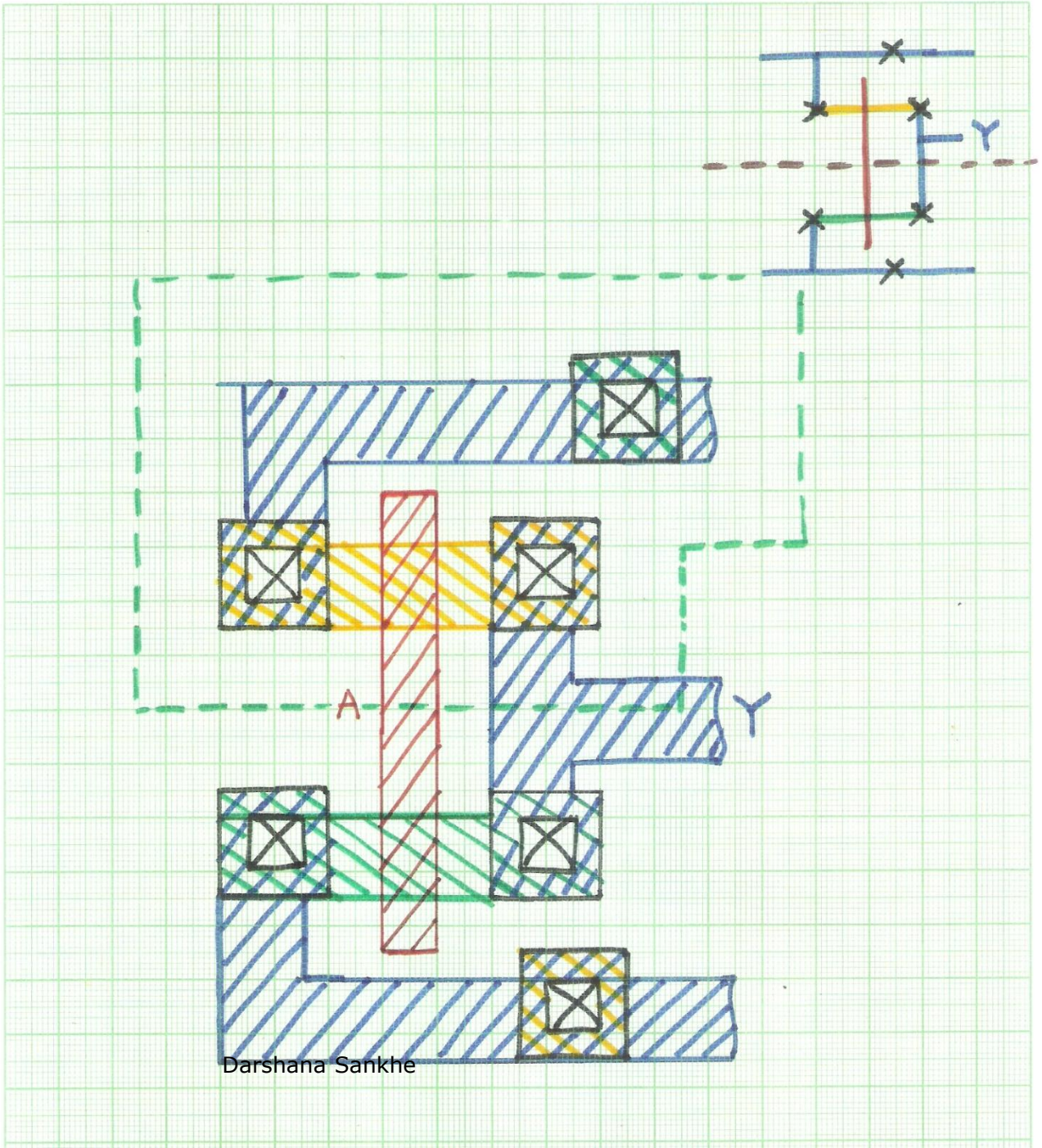
- Line size and spacing:
  - **metal1:**
    - Minimum width=3λ, Minimum Spacing=3λ
  - **metal2:**
    - Minimum width=3λ, Minimum Spacing=4λ
  - **poly:**
    - Minimum width= 2λ, Minimum Spacing=2λ
  - **ndiff/pdiff:**
    - Minimum width= 3λ, Minimum Spacing=3λ,
  - **wells:**
    - minimum width=6λ,
      minimum n-well/p-well space = 6λ(They are at same potential)
      = 9λ (They are at different potential)

Design Rules: CMOS

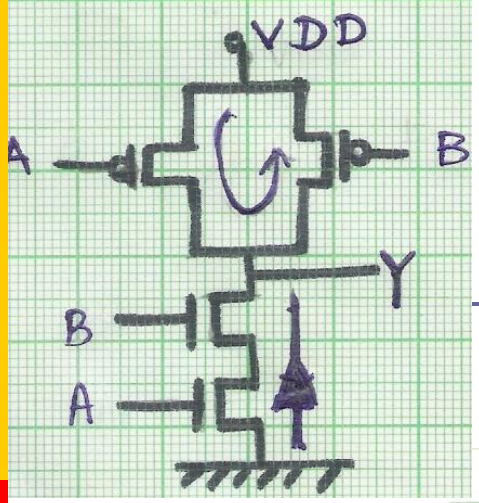
- Transistors:
  - Min width=3λ
  - Min length=2λ
  - Min poly overhang=2λ

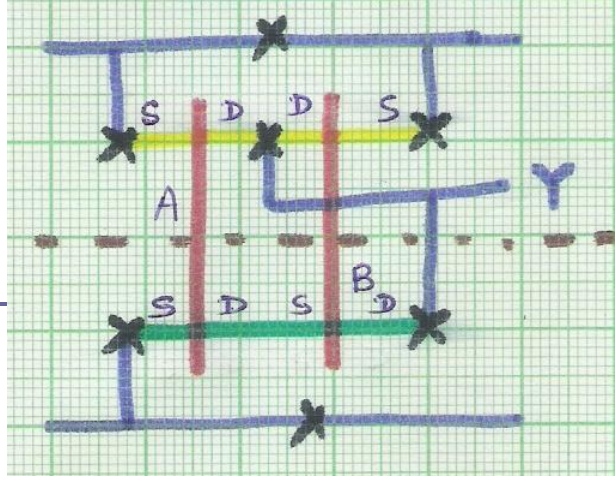
- Contacts (Vias)
  - Cut size: exactly 2λ X 2λ
  - Cut separation: minimum 2λ
  - Overlap: min 1λ in all directions

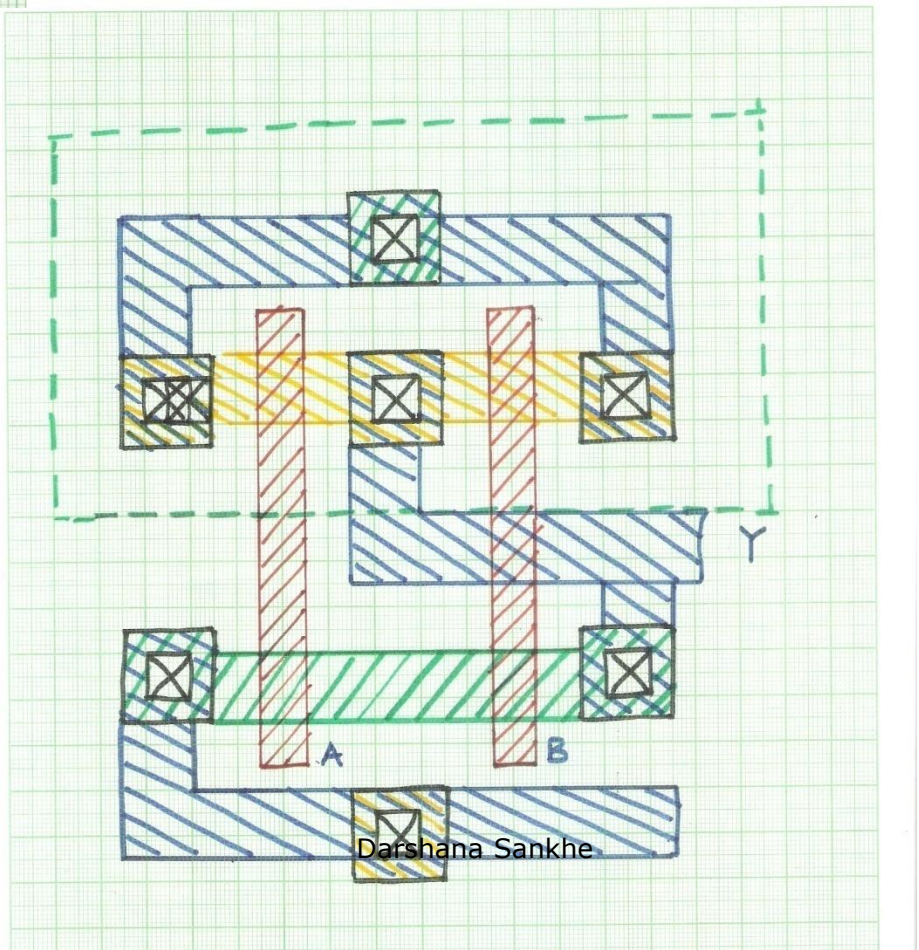
CMOS Inverter:



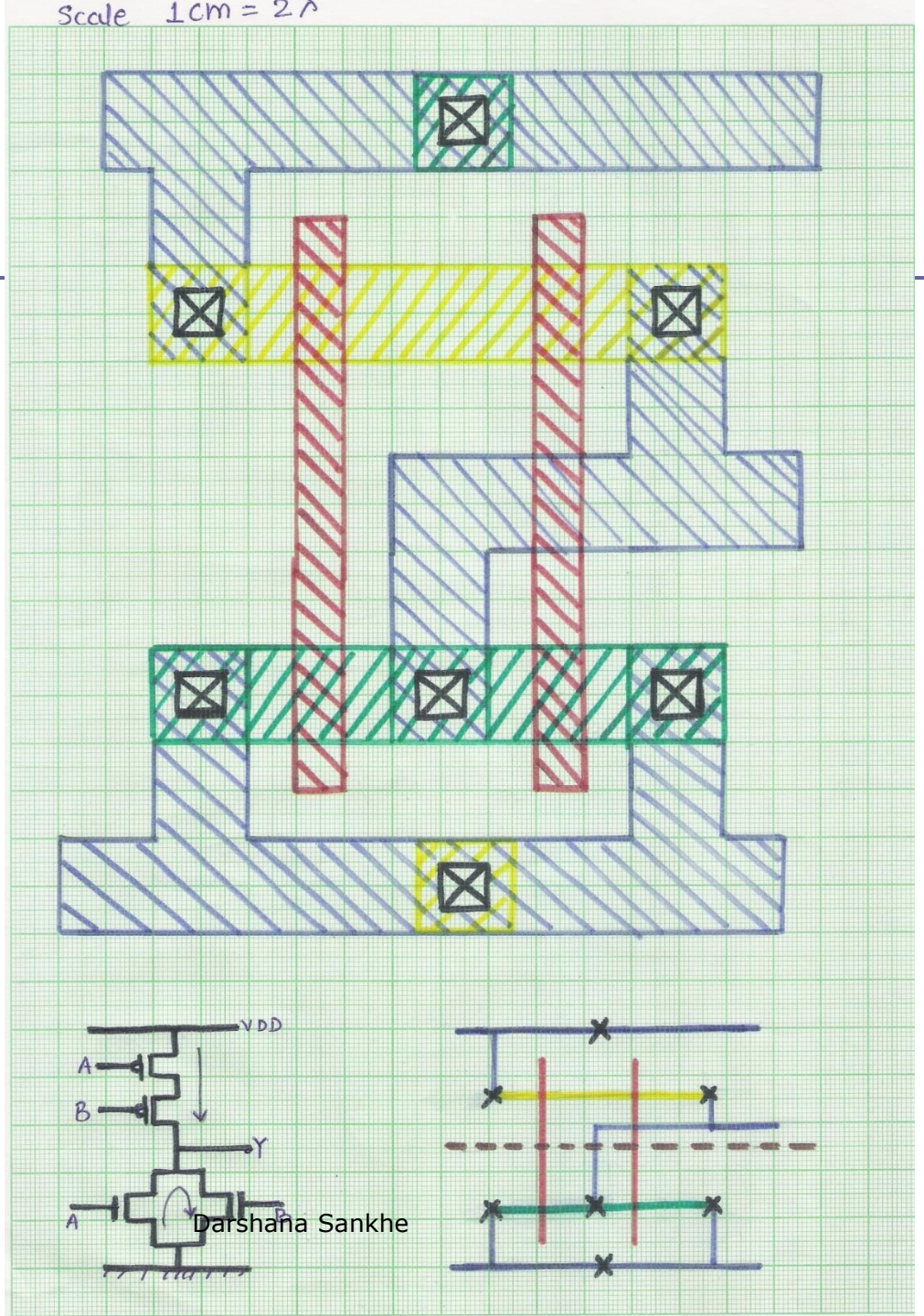
CMOS NAND





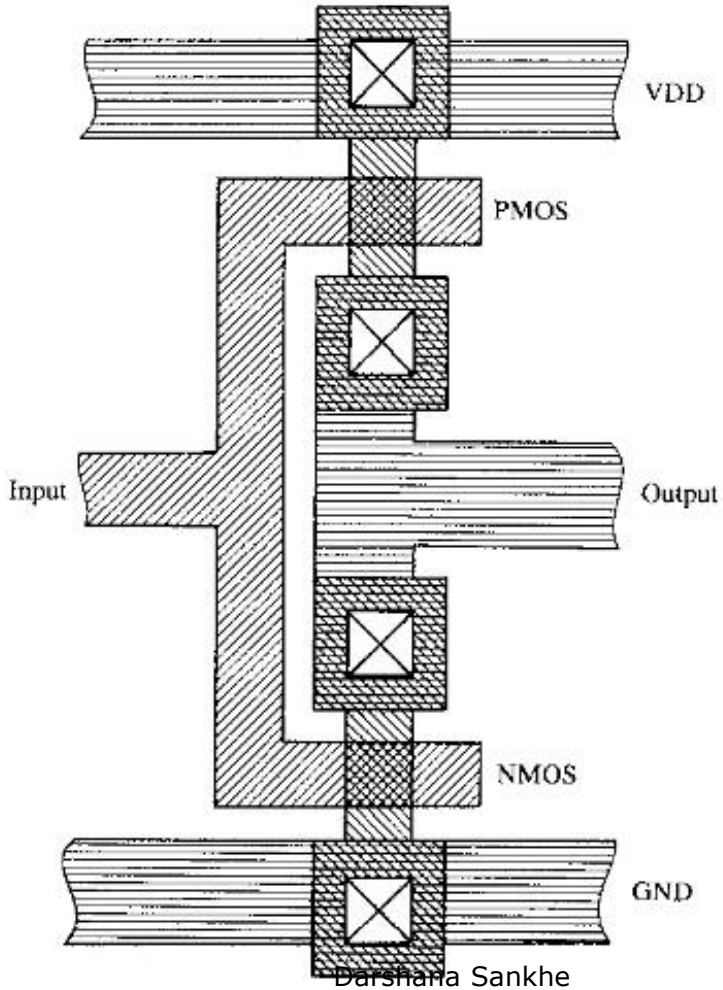


CMOS NOR :



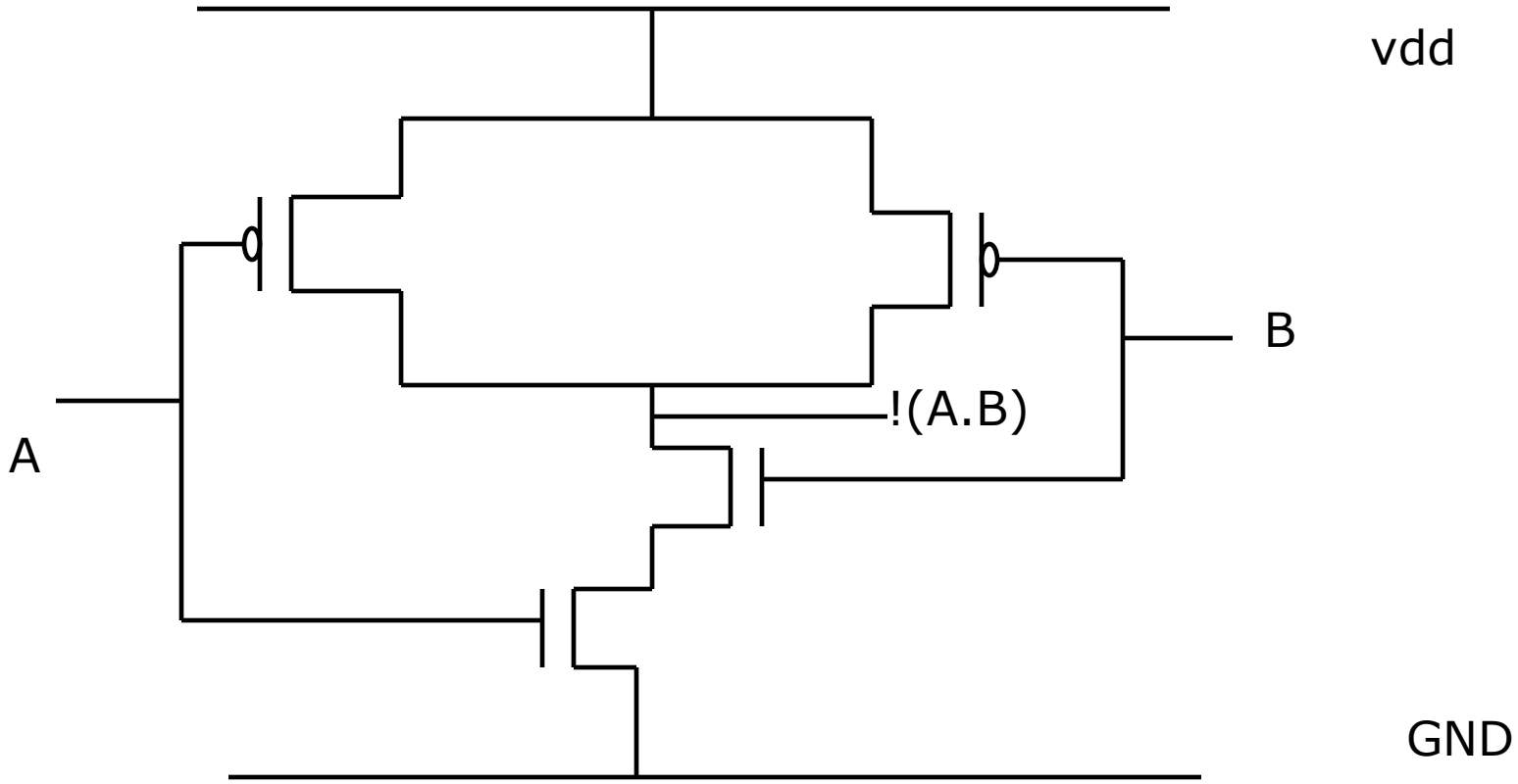
CMOS INVERTER

(This layout does not have n-well and contacts for n-well and substrate)



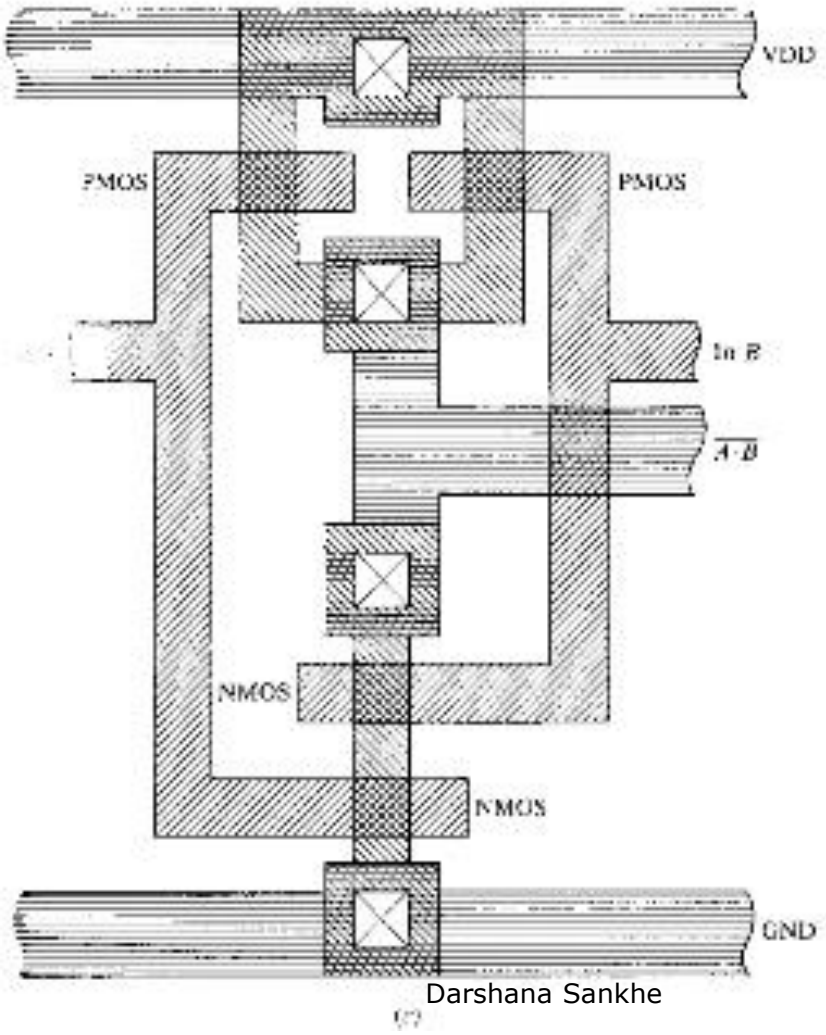
(c)

CMOS NAND

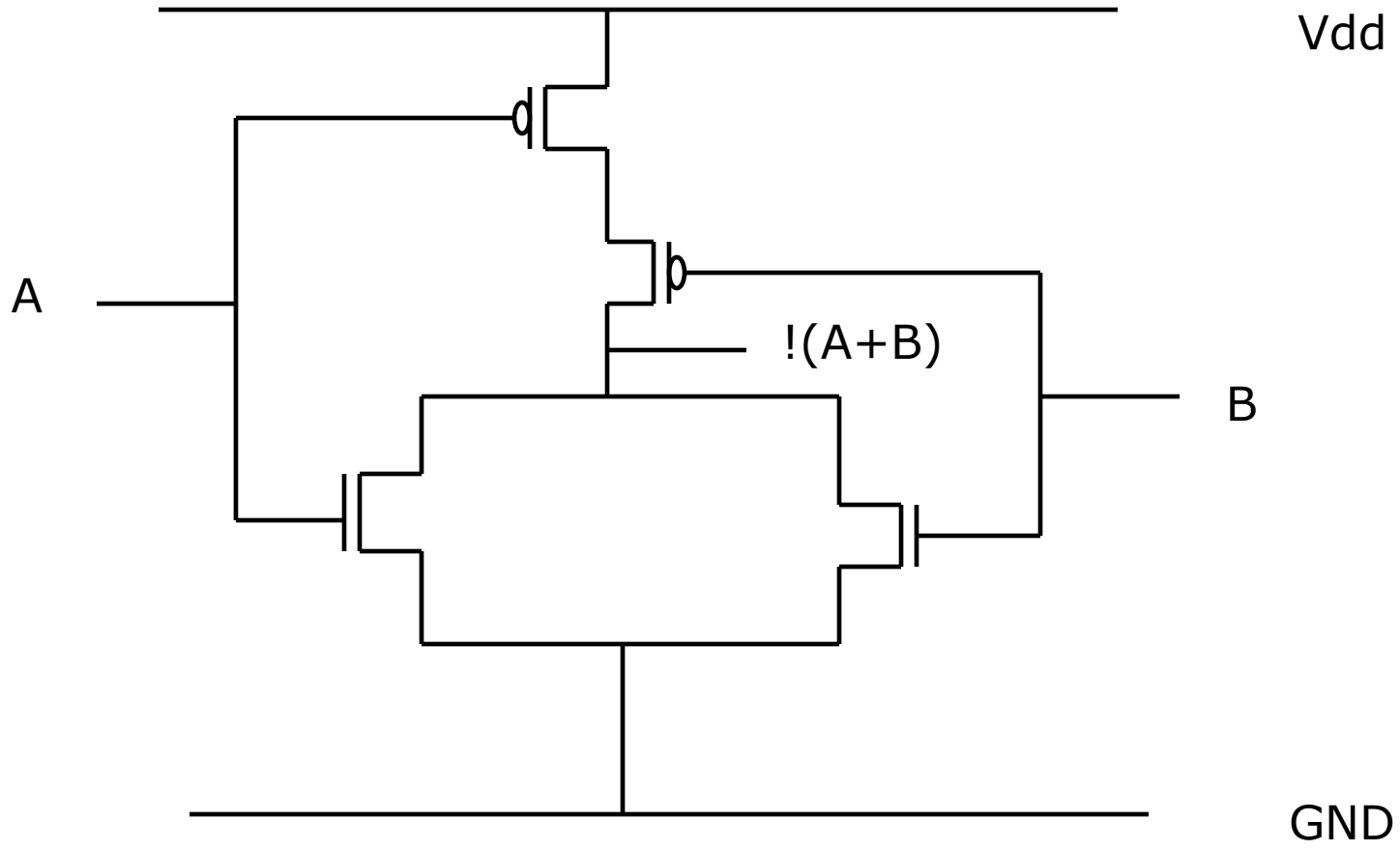


CMOS NAND

This layout does not have n-well and contacts for n-well and substrate)

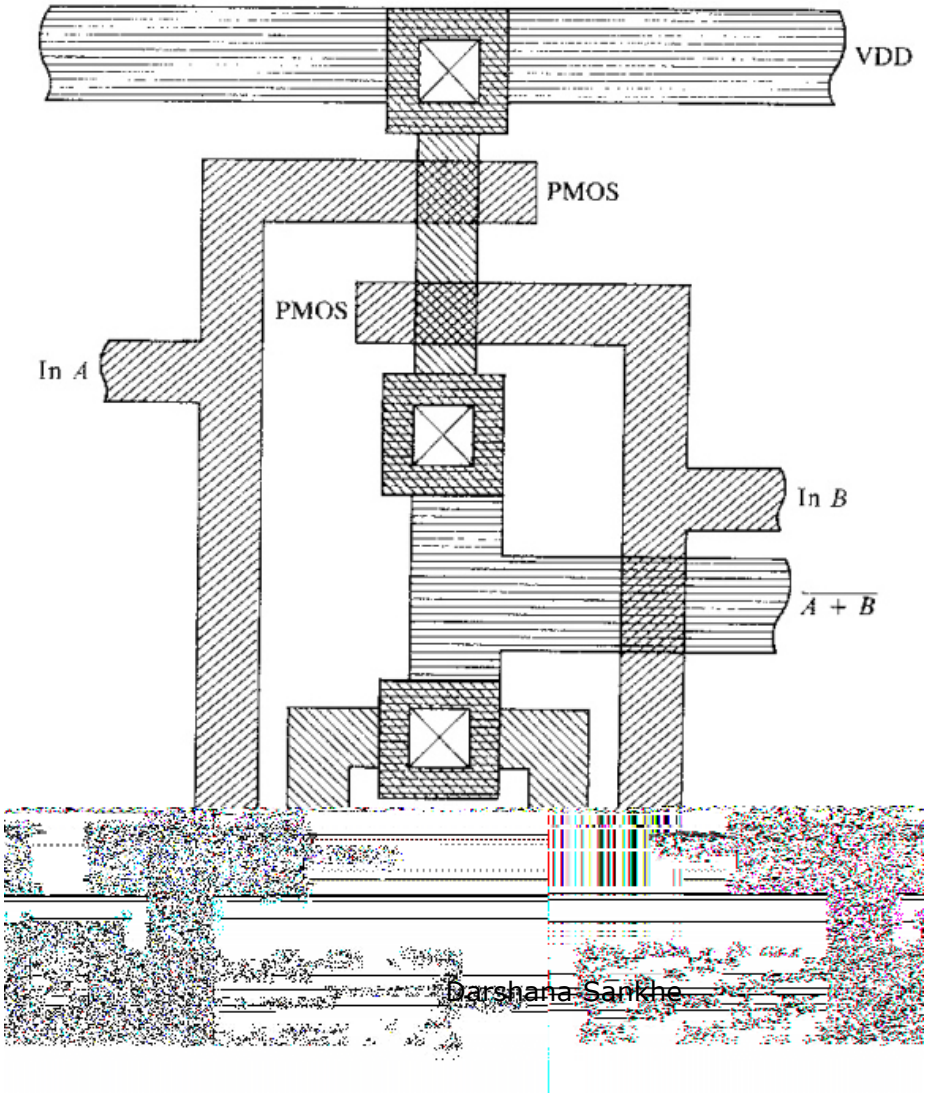


CMOS NOR(Circuit Diagram)



CMOS NOR

This layout does not have n-well and contacts for n-well and substrate)



Design of NMOS/CMOS Circuits:

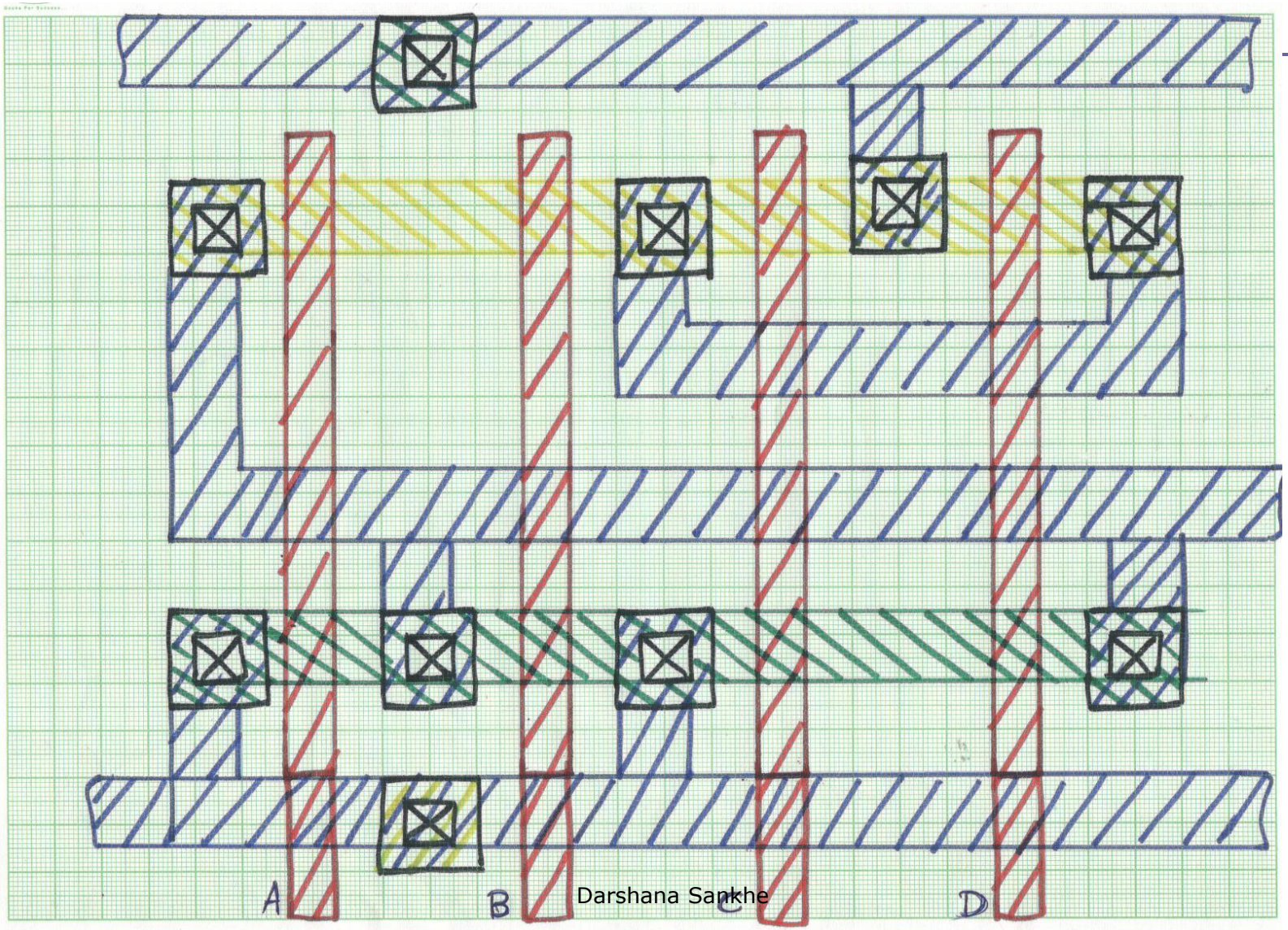
- PDN – The Function to be implemented, must be expressed in a inverted form.

- $F = \overline{(A + BC)\, D}$

- $F = (AB + C)(D + E)$

- $\overline{F} = A + B + CD$

F’ = A + B + CD



Thank you