COMPARISON BETWEEN MESA ISOLATION AND P+ IMPLANTATION ISOLATION FOR 4H-SiC MESFET TRANSISTORS

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Abstract–*Silicon Carbide (SiC) is considered the wide band gap semiconductor material that can presently compete with silicon (Si) material for power switching devices.*

Progresses in the manufacturing of high quality SiC substrates open the possibility to new circuit applications. SiC unipolar transistors, such as JFETs and MESFETs have also a promising potential for digital integrated circuits operating at high temperature and/or in harsh environments.

An increasing demand for high temperature compliant circuits comes from intelligent power management, automotive industry, and intelligent sensors for harsh environment, space and aerospace as well.

Mesa isolation is a widely used isolation technique for the definition of individual devices due to its simplicity as fabrication process [1]. It is mostly used for the protection of high power devices.

The junction isolation is widely used for bipolar, Bi-CMOS integrated circuits (IC) and can be achieved by diffusion or implantation process.

The present work is presenting the experimental comparison between the mesa isolation process and p+ implantation junction isolation for 4H-SiC MESFET transistors.

Keywords: *4H-SiC, P+ implantation, mesa etching, JFET, MESFET, SiC integrated circuits.*

1. INTRODUCTION

Wide band gap semiconductors (WBG) have properties such as high breakdown voltage, high temperature operation capability, and high thermal conductivity, making them potentially superior to Silicon (Si) semiconductors and thus making them attractive for a new generation of electronic devices.

Among the various WBGs, 4H-SiC (Silicon Carbide) poly-type is the most promising material for power switching device applications due to their inherent material characteristics, quality of the crystal growth, and the maturity of manufacturing process. 4H-SiC MESFET, particularly, has the capability of high voltage, high temperature, high thermal conductivity and harsh radiation environment operation.

Due to the recent progress in device process and the technology for producing high quality SiC substrates and epitaxial films, impressive performances for SiC MESFETs has been reported.

The definition (in area and depth) of active devices in semiconductor material has been a major process requirement for the advances made in the integrated circuits (ICs) revolution. The definition of discrete individual devices, and the separation of devices on the same piece of material (integration), is normally achieved through either material removal (etching) and/or junction isolation (diffusion/implant). Another challenge consists in the reduction of the number of fabrication steps combined with high production yield of the complete final devices and circuits.

The research presented in this paper has focused on the two isolation process for the 4H-SiC MESFET transistors.

2. DESIGN AND FABRICATION

The mesa isolation technique is attractive because of its simplicity and consists of patterning the semiconductor into islands or “mesas” using a mask step and a semiconductor etch step.

Ion implant is a widely used technique for the WBG semiconductor doping. The diffusion technique in SiC has not shown relevant results for the poly-type 4H-SiC, therefore for the pattern device junction isolation has been used p+ implantation.

The two type MESFET devices presented in this work were fabricated on 4H-SiC wafers supplied by CREE Research Inc. The P layer grown on a semi-insulating substrate has a 5µm thickness with $5\times1015cm^{-3}$ doping

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concentration and the N layer has 0.5µm thickness with a doping concentration of 1017cm^{-3} (Fig.1, Fig.2).

The first type of 4H-SiC MESFET is isolated using mesa etching and the second one using p+ implantation.

In order be able to have a cogent comparison between the two devices, the W/L ratio of the mesa MESFET is 10 times higher than the junction isolated device with m=1.

In the following part it will be briefly described the device fabrication concerning the impact of the two processes on the substrate and on the electrical characteristics of de device.

2.1. Mesa Isolation

The fabrication of 4H-SiC MESFET transistor using mesa isolation was already reported in [2] as having a proper behavior up to an ambient of 200ºC. In our previous work [3 were reported results up to 300ºC.

The technology used for the fabrication of these devices is a multi-device process with 8 levels of photolithography masks [4], including the mesa etching isolation process. The general design of the MESFETs is presented in Fig.1.

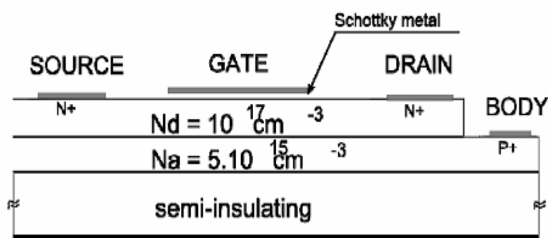

Fig. 1. Schematic cross-section of the 4H-SiC MESFET with mesa isolation.

The mesa etching was achieved in a standard RIE process through a patterned deposited SiO2.

The fabrication process also includes ion-implantation and impurity temperature activation, field oxide formation, ohmic contact formation, gate contact definition, and pad metallization. This technology allows integrating LJFET, Schottky, JBS and PiN diodes and small signal NPN bipolar transistor. It is also possible to integrate large value resistors with a reasonably small footprint thanks to the lightly doped P layer.

2.2. Isolation by P+ Implantation

In order to fabricate ICs on 4H-SiC we have used another isolation method, the junction isolation technique that provides a better planarization of the surface.

This isolation method is mostly used for the design and fabrication of ICs on Si. Since a number of devices are to be fabricated on the same IC chip, it becomes necessary to provide good isolation between various component and their interconnections.

A benefit of using p+ implantation isolation process is the improvement of the density of devices per unit area and wafer surface.

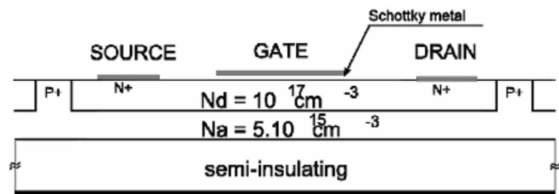

Fig. 2. Schematic cross-section of the 4H-SiC MESFET with p+ implant isolation.

The p+ implantation isolation process is a PN junction isolation technique. The p+ type impurities are deeply implanted into the N-type epitaxial layer through a metal mask so that it touches the P-type substrate at the bottom (Fig.2). This method generated n-type isolation regions surrounded by p-type moats.

If the P-substrate is held at the most negative potential, the diodes will become reverse-biased, thus providing isolation between these islands. The individual components are fabricated inside these islands.

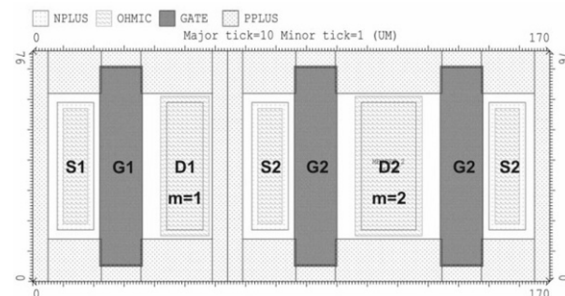

Fig. 3. Layout of different multiplicity MESFETs isolated with p+ ring implantation used in digital ICs.

In Fig. 3 is presented the layout design of the proposed MESFET transistors isolated by implanted pn junction. In the left side is presented the MESFET with multiplicity 1 and

in the right side is one with multiplicity 2. As can be seen the devices are isolated between using a p+ implantation wall. This approach was used for developing 4H-SiC digital integrated circuits with N-type epitaxial resistors on the same chip [3], [5].

The design geometry used for the devices using the p+ implantation wall is different than the one used before in order to use the concept of transistor multiplicity.

This technology also allows integrating LJFET, Schottky, JBS and PiN diodes, small signal NPN bipolar transistor and also realization of N-type resistors.

3. EXPERIMENTAL RESULTS

The MESFET devices using the two different types of isolation were fabricated on 4H-SiC (Fig.4 and Fig. 5).

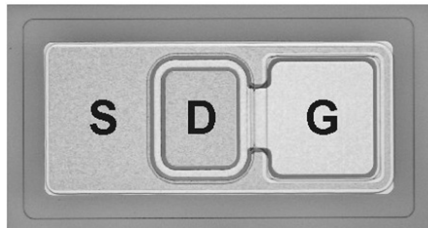

Fig. 4. 4H-SiC MESFET fabricated device with mesa isolation.

An important aspect in order to be able to develop ICs on SiC is the necessity of having scalable transistors. Though mesa etching assures a good isolation of the devices, using this method of device isolation makes difficult to create scalable transistors.

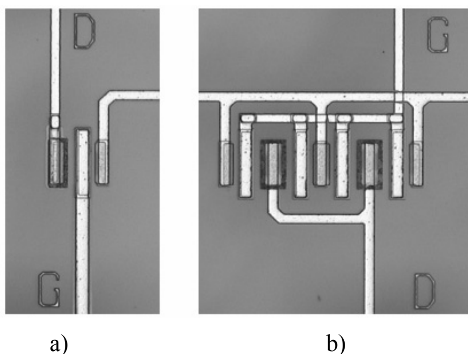

Fig. 5. 4H-SiC MESFET (a) m=1 and (b) m=4 using p+ implantation isolation wall.

In Fig. 4 is presented the fabricated transistor isolated with mesa etching and in Fig. 5 are presented two MESFET devices having different orders of multiplicity (m=1 and m=4) in order to show the scalability of the devices.

The device isolation using mesa etching is used for either high power or low power devices, but this method for ICs presents some inconvenient.

Mainly because of the etching process, the planarity of the wafer it is not appropriate between different levels of metallization. The planarization techniques existent for silicon wafers are not adaptable for SiC ones.

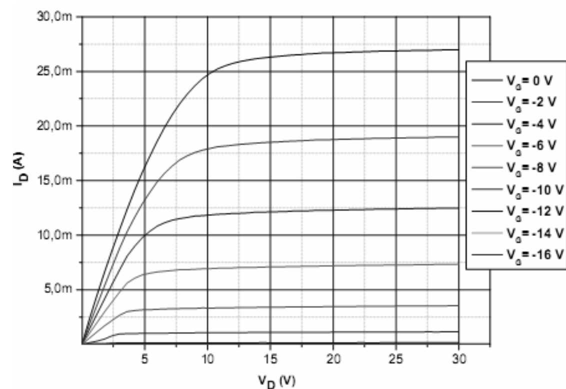

Fig. 6. The $I_D(V_D)$ characteristics of the MESFET isolated with mesa etching.

The transistors were characterized at room temperature and the DC characterization was achieved using two Keithley SMUs.

As can be seen in Fig. 6 from the experimental DC characteristics of the 4H-SiC MESFET (Fig. 4) isolated using mesa etching process, shows a very good behaviour.

From the DC characteristics (Fig. 6 and Fig. 7a) extracted from measurements made on both types of MESFETs (Fig. 4 and Fig. 5a), it can be easily seen that the drain current of the mesa transistors is roughly x10 times higher than of the transistor isolated using p+ implantation. The results are in a good agreement taking into account that the two compared devices are fabricated on different wafers.

In Fig. 7 are presented the electrical characteristics of the MESFET transistors isolated with pn junction, with two different order of multiplicity (m=1 and m=4) (Fig. 5).

From the experimental plots presented in Fig.7 it is easy to observe that the drain currents ratio between the two devices is the

same number with the multiplicity order of the transistors (m=4).

For V_D=30V at V_G=0V, I_D(m=1)=2mA and respectively I_D(m=4)=8mA. The scalability is demonstrated for all orders of multiplicity of the transistors.

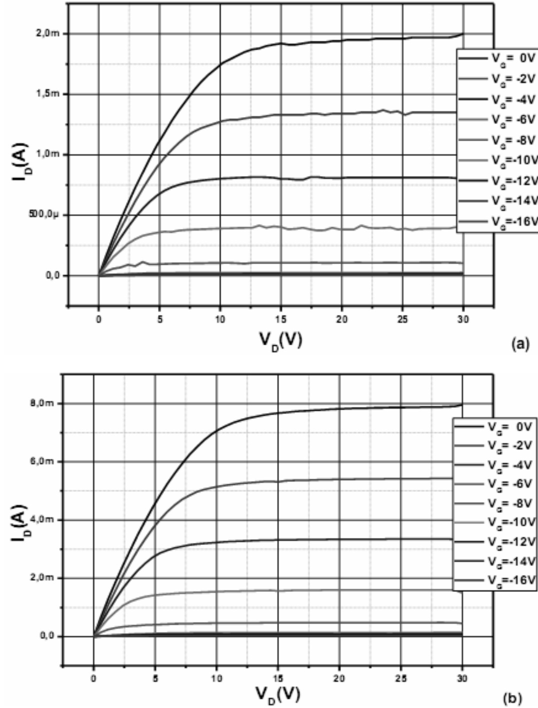

Fig. 7. The $I_D(V_D)$ characteristics of the MESFET isolated with p+ implantation wall for (a) m=1 and (b) m=4 multiplicity.

Nevertheless, the transistor geometry from Fig.3 has a built in a drain-source residual current. In order to minimize it, was created ageometry trick on the lateral extremity of the gates. Thus, the value of the residual current is more than 500 times smaller than the main drain current.

At high temperature operation, the residual current of the transistor is decreasing because the on-resistance is increasing with temperature.

Though the residual current can be presented as a disadvantage, it does not affect the functionality of logic integrated circuits.

4. CONCLUSIONS

In this paper, we have presented the experimental comparison between the mesa isolation process and pn junction isolation by p+ implantation for 4H-SiC MESFET transistors. The p+ implantation transistors were designed with parameters extracted from already fabricated MESFETs with mesa isolation.

We have demonstrated that 4H-SiC MESFETs isolated by pn junction are feasible for SiC approach, as well as the possibility to produce scalable MESFETs transistors having in a good agreement with mesa etch isolation.

The advantage of p+ implant junction isolation is the avoiding of the steps on semiconductor surface, which are inherent for mesa isolation. These steps are known as responsible for the discontinuity of interconnection metal traces, and one of the failure mechanisms of complex circuitry. By using the p+ implantation junction isolation, these issues are avoided.

As our knowledge, this is the first tentative of using device isolation using p+ implant junction isolation. The 4H-SiC MESFET transistors here presented are being further used in integrated circuits with logic gates [3], [5].

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