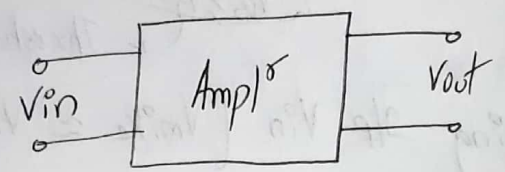
Module 5.3: E-MOSFET Small Signal AC Analysis (E-MOSFET amplifier)

01
7/11/19

- **Amplifier requirements:**

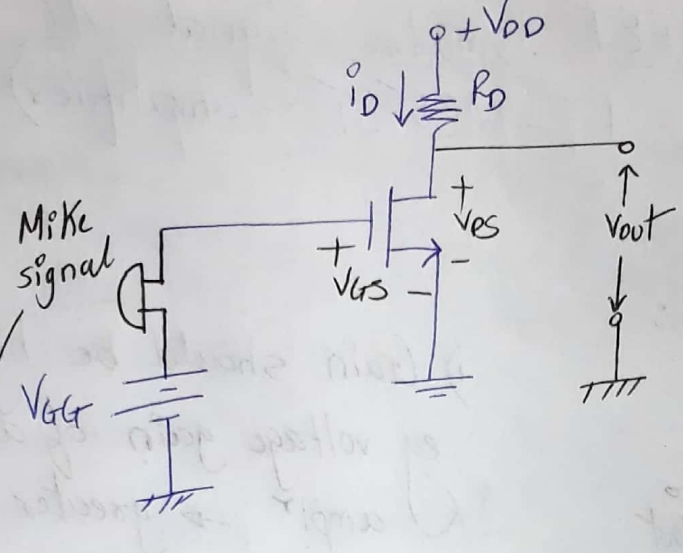


1) Gain should be high
   eg voltage gain of a voltage ampl^r → greater than 1
2) I/p impedance
3) o/p impedance
4) Linearity (o/p should be Linear w.r.t I/p)

- Enhancement-MOSFET as a device should amplify
  → small-time varying signals.

This condition must be satisfied for MOSFET amplifier to be **Linear**

- Next, we need to superimpose small AC s/g with DC?
  Why DC biasing is required → so that MOSFET wakes up & works in proper mode ie saturation → so that it is used as amplifier



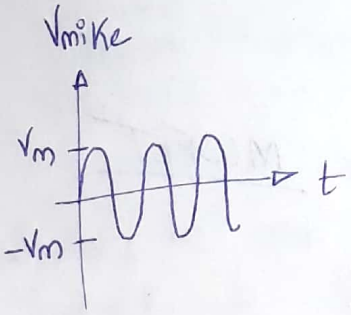
Note: why connect V_{GG}?
To bias MOSFET in saturation region, such that $V_{GS} \geq V_T$
↳ Threshold voltage

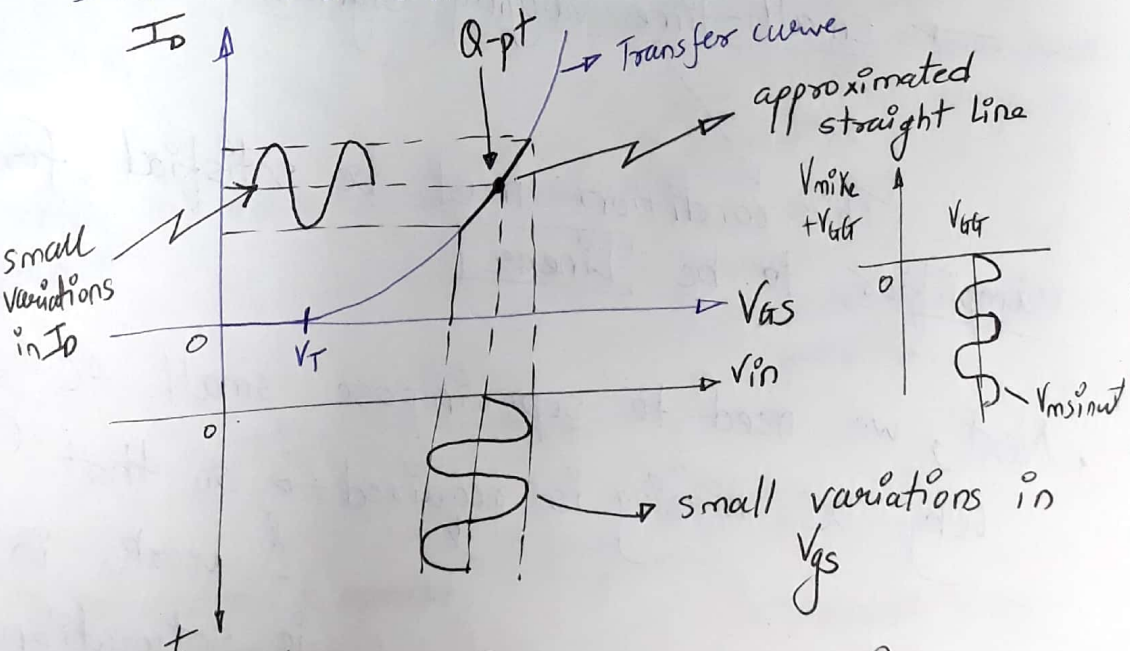
It acts as a small time-varying I/p Vin ($V_{mike} \simeq V_m \sin\omega t$)

→ MOSFET acts as : voltage-dependent current source

↳ "converts" a voltage to a current
(V_{GS}) or V_{gs}
(I_D) --- DC quantity
(i_d) --- AC quantity

↳ It's a V-I converter ie Transconductor





small variations in V_{gs}

→ Here, the idea is to consider small segment of exponent curve to be linear

So, our I/p sig limit should be within this linear segment (called as small-sig)

Hence Combining transfer curve of MOSFET & time response of I/p

· Concept of transconductance

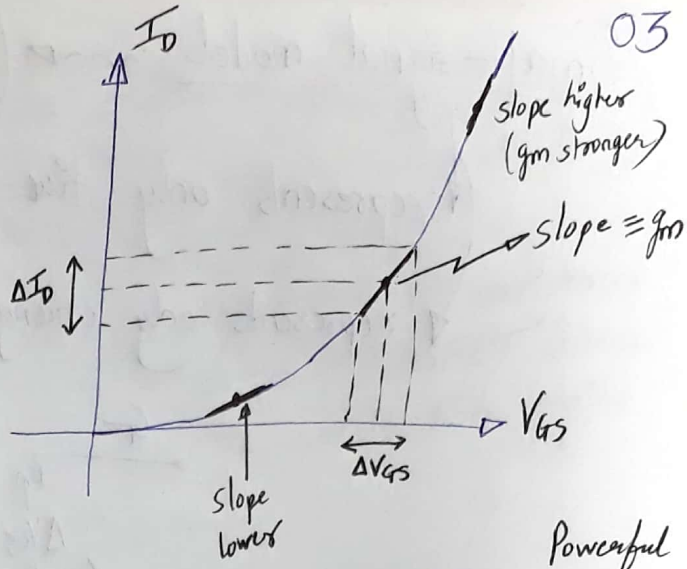
From graph,

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{Q\text{-pt}}$$

slope of I_D vs V_{GS} characteristics

Unit: $\frac{1}{\Omega}$ or $\frac{mA}{V}$

ie $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$



$$I_D = K_n (V_{GS} - V_T)^2$$

$$\frac{dI_D}{dV_{GS}} = 2K_n (V_{GS} - V_T)$$

$$\boxed{g_m = 2K_n (V_{GS} - V_T)}$$ ---- Mathematically

$\Rightarrow$ $\boxed{\Delta I_D = g_m \Delta V_{GS}}$ --- Powerful concept

- ΔI_D: Small changes in I_D
- g_m: slope, a constant
- ΔV_{GS}: Small changes in V_{GS}

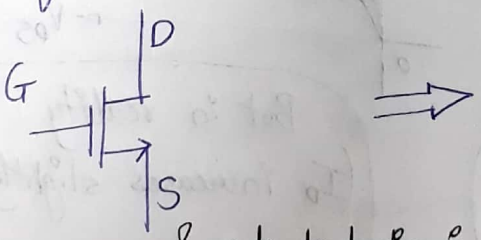
It suggest that gate to source voltage controls the drain to source current in a MOSFET.

Now, we are ready to draw small-signal model of MOSFET

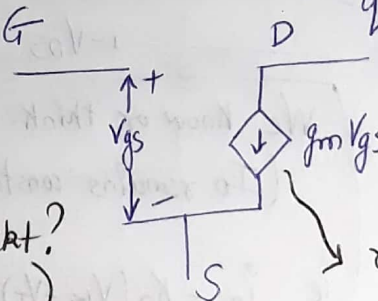
$v_{gs} = \Delta V_{GS}$
$i_D = \Delta I_D$

Δ means small changes in

represents time-varying quantities



$\Rightarrow$



represents change in I_D

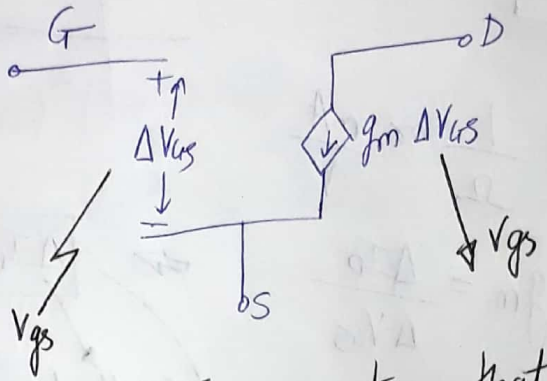
ie $\boxed{\Delta I_D = g_m \Delta V_{GS}}$

→ Gate to source & gate to drain is open ckt?

I/p impedance of MOSFET is v.high, since metal Gate is separated from S & D by an oxide layer

Small-signal model ⇝ (represents only time-varying quantities) Ot

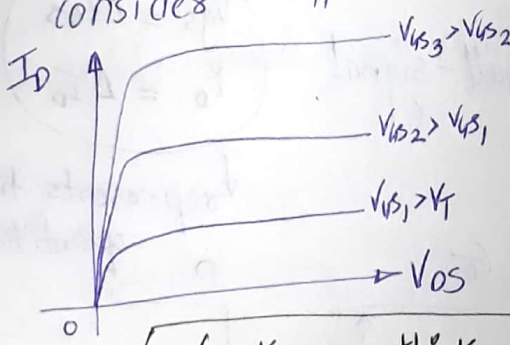
- represents only time-varying components
- represents only changes in parameters (voltage V_{gs}, current i_D)



Small-slg model of JFET suggests that the drain current fluctuations (ΔI_D) is equal to V_{GS} fluctuations (ΔV_{GS}) times the slope (g_m)

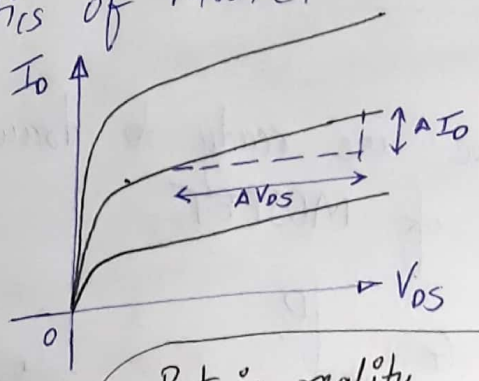
- **Small-slg o/p resistance/impedance (r_o or r_d):**

let's consider o/p characteristics of MOSFET



We know or think (I_D remains constant)

ie $i_D = K_n (V_{GS} - V_T)^2$



But in reality (I_D increases slightly with V_{DS})

$i_D = K_n (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$

λ – channel length modulation parameter

From graph, $(I_D - V_{DS})$

$$\text{Slope} = \frac{\Delta I_D}{\Delta V_{DS}}$$

$$\boxed{\frac{1}{\text{slope}} = \frac{\Delta V_{DS}}{\Delta I_D} = r_o \text{ or } r_d}$$

small-sig o/p resistance of a MOSFET biased in saturation region

ie $I_D = K_n (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$

$$\frac{dI_D}{dV_{DS}} = \lambda K_n (V_{GS} - V_T)^2 = \lambda I_{DQ}$$

ie $\frac{dI_D}{dV_{DS}} = \lambda I_{DQ}$

ie $\frac{dV_{DS}}{dI_D} = \frac{1}{\lambda I_{DQ}}$

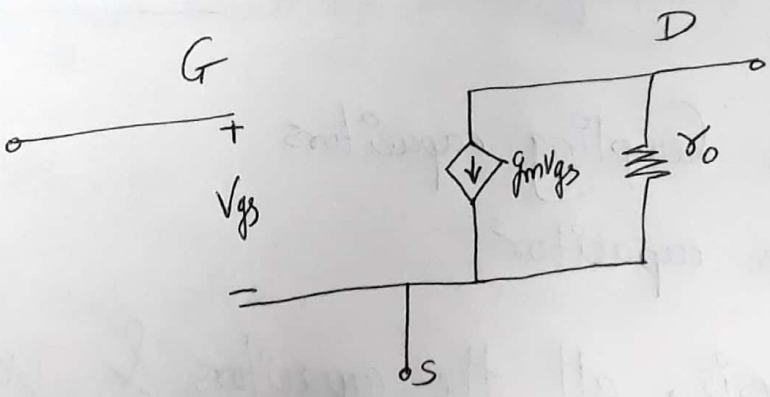
ie $\boxed{r_o \text{ or } r_d = \frac{1}{\lambda I_{DQ}}}$

small-sig o/p resistance

We need to include this r_o in small sig model, (we connect r_d betn DDs)

Complete small-sig model of E-MOSFET n-channel

Congratulations

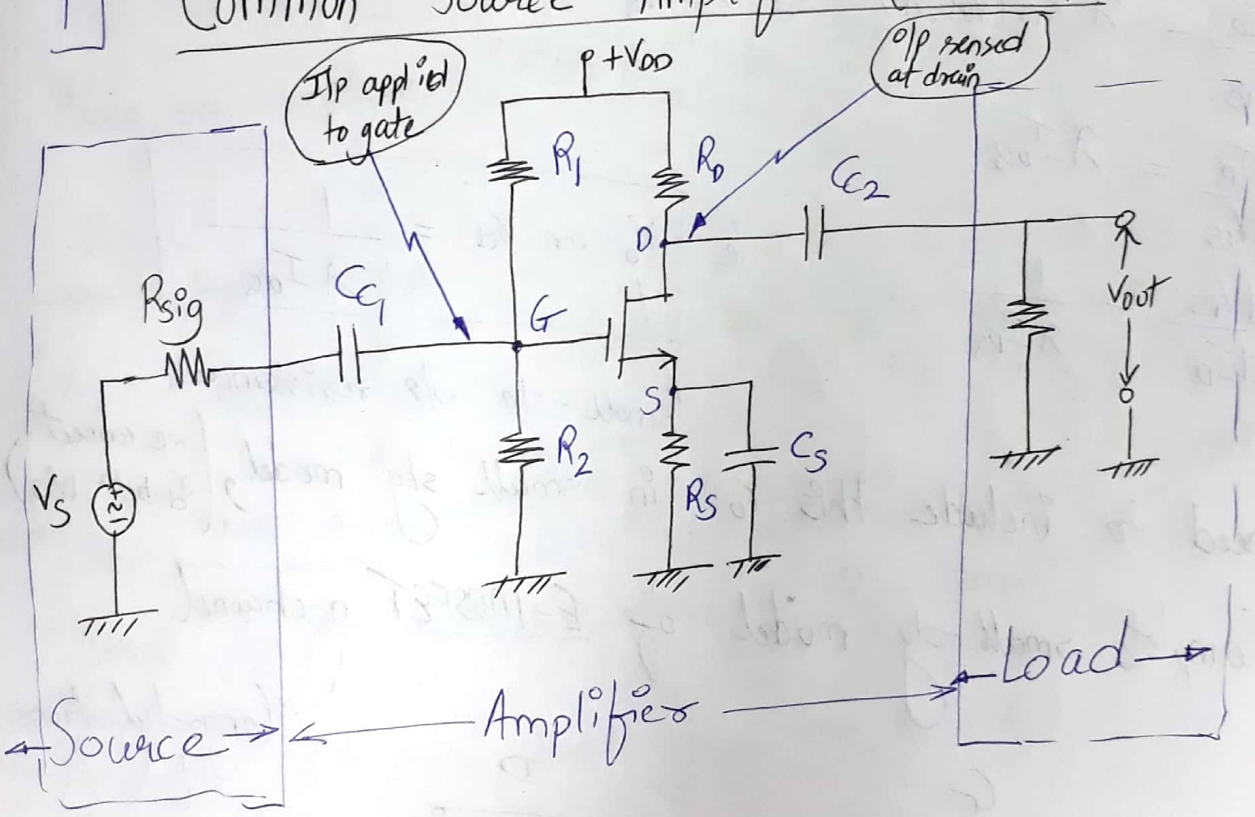


We finally have a small sig model of MOSFET

• MOSFET amplifier configurations:- (NMOS-E)

1. Common source (CS) amplifier
2. Common gate (CG) amplifier
3. Common drain (CD) amplifier or Source follower

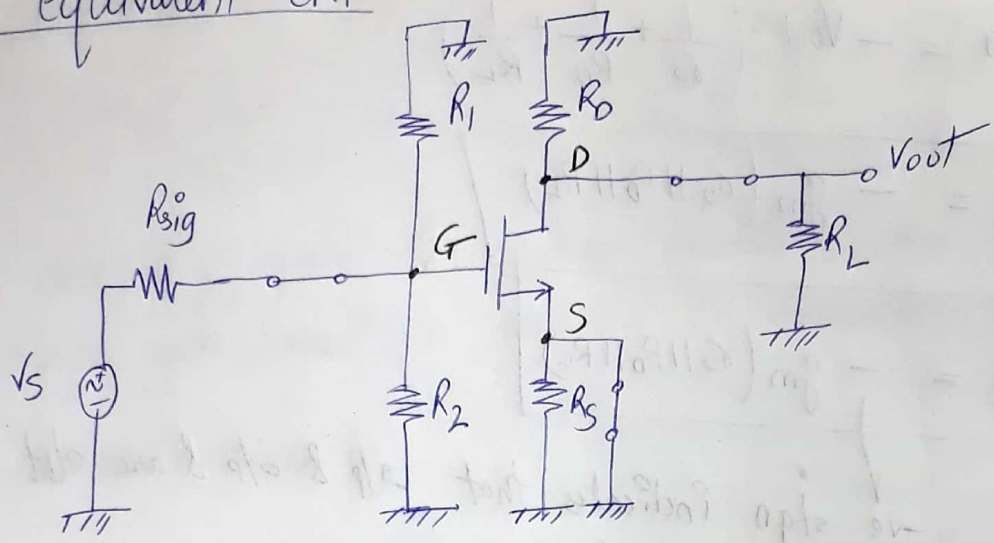
1] Common Source Amplifier (NMOS-E) :-



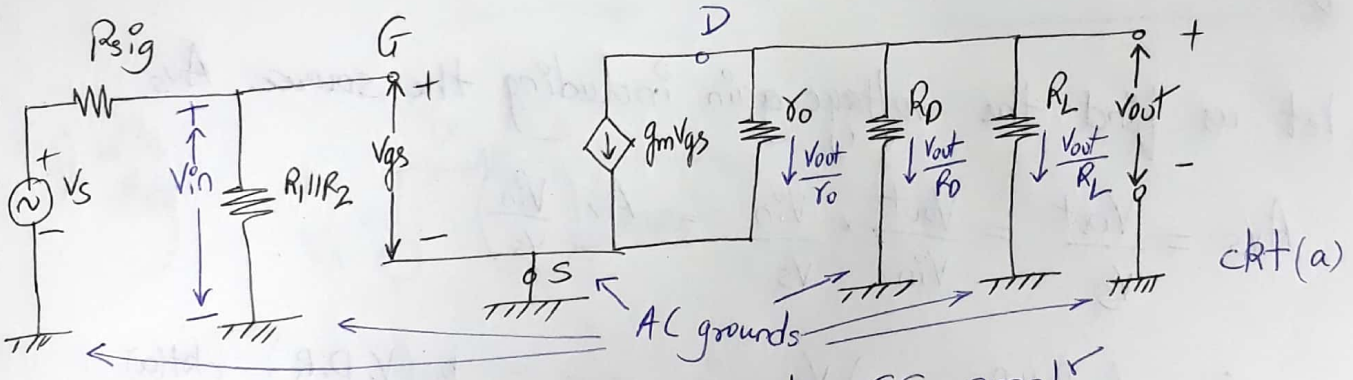
- C_{C_1} & C_{C_2} : Coupling capacitors
- C_S : Bypass capacitor

→ For AC analysis, all the capacitors & DC supply is replaced by a short-circuit.

AC equivalent ckt



Now, we replace **MOSFET** by its small-s/g model



Small-s/g AC equivalent ckt of CS ampl^r

Analysis: (to find small-s/g voltage gain A_v)

From ckt(a), $V_{in} = V_{gs}$

→ KCL at 'D' node gives,

$$g_m V_{gs} + \frac{V_{out}}{r_d} + \frac{V_{out}}{R_D} + \frac{V_{out}}{R_L} = 0$$

ie $g_m V_{in} = -V_{out}\left(\frac{1}{r_o} + \frac{1}{R_D} + \frac{1}{R_L}\right)$

$$\frac{V_{out}}{V_{in}} = -g_m(r_o \| R_D \| R_L)$$

ie $$A_v = -g_m(r_o \| R_D \| R_L)$$

-ve sign indicates that i/p & o/p are out of phase with each other.

→ If r_o & R_L are not present, then $A_v = -g_m R_D$

Now, let us find the voltage gain including the source A_{vs}

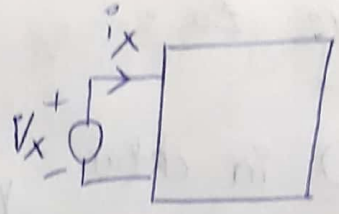
$$A_{vs} = \frac{V_{out}}{V_s} = \frac{V_{out}}{V_{in}} \times \frac{V_{in}}{V_s} = A_v\left(\frac{V_{in}}{V_s}\right)$$

→ $V_{in} = \left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_{sig}}\right) V_s$ ---- by (V.D.R) ckt(a)

ie $$A_{vs} = A_v\left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_{sig}}\right)$$

The term "$\left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_{sig}}\right)$" is the attenuation factor

I/p impedance :- Z_i

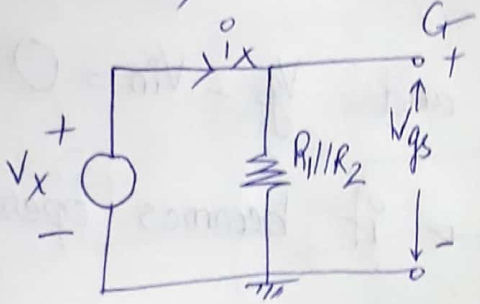


$$Z_i = \frac{V_x}{i_x}$$

In ckt (a), gate & source terminal are open-circuited, since gate current in MOSFET is v.v small ($I_G \approx 0$)

→ ckt (a) reduces to,

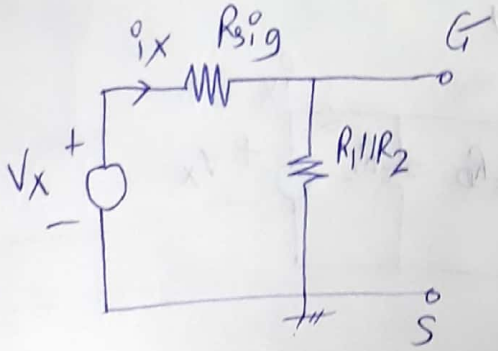
1) without R_{sig}



$$Z_i = \frac{V_x}{i_x}$$

$$\boxed{Z_i = R_1 \| R_2}$$

2) with R_{sig}



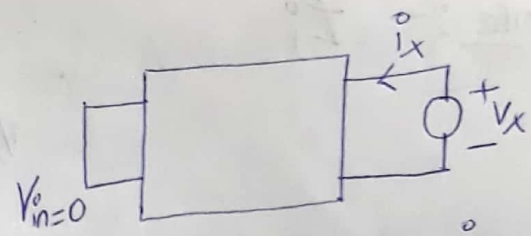
$$Z_{is} = \frac{V_x}{i_x}$$

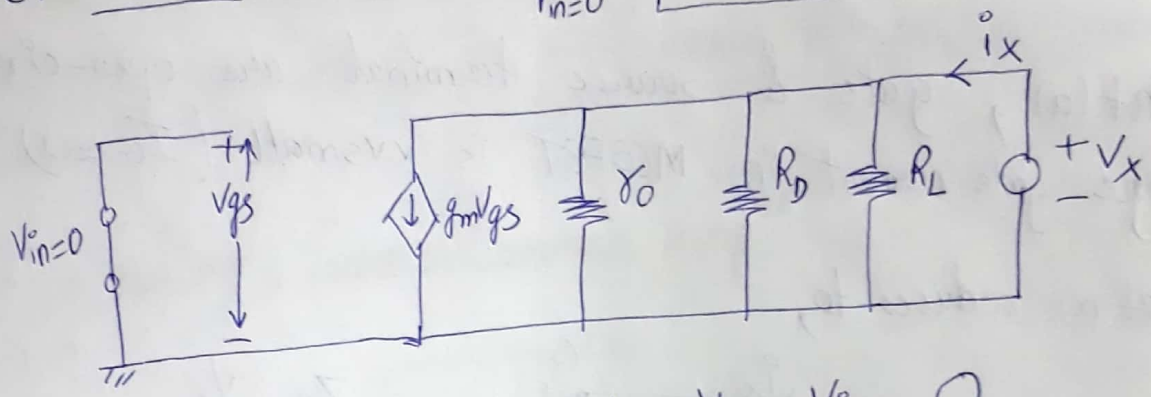
$$\boxed{Z_{is} = R_{sig} + R_1 \| R_2}$$

↳ I/p impedance with R_{sig}

Output impedance Z_o :-

Set $V_{in} = 0$ in ckt(a)

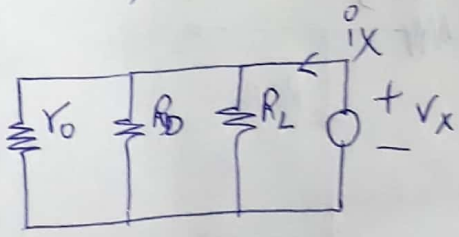




→ Since $V_{in} = 0$; and $V_{gs} = V_{in} = 0$

$g_m V_{gs} = 0$ → it becomes open ckt

Circuit (a) reduces to,



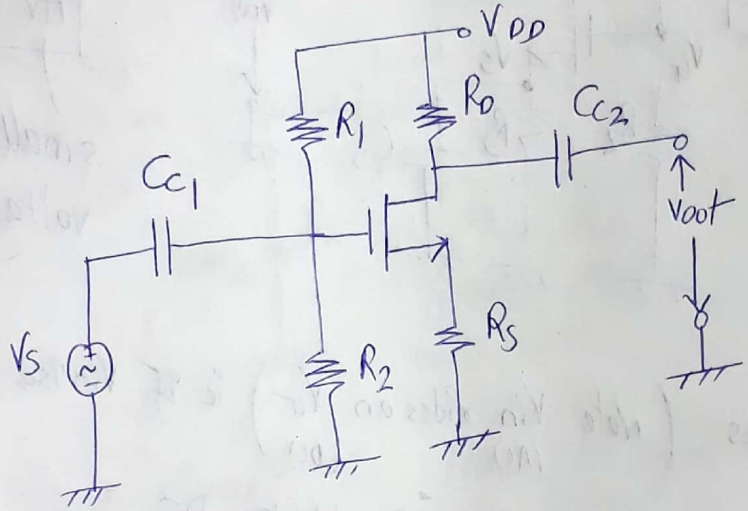
$$\frac{V_x}{i_x} = r_o \,||\, R_D \,||\, R_L$$

$$\boxed{Z_o = r_o \,||\, R_D \,||\, R_L}$$

o/p impedance

Note: Small-sig AC analysis of MOSFET is **SAME** as that of JFET.
(Only difference is in the a) Formula of g_m b) Symbol for MOSFET & JFET)

* Degenerated Common source ampl^r



Here,
$\lambda = 0$ ie $r_o = \infty$

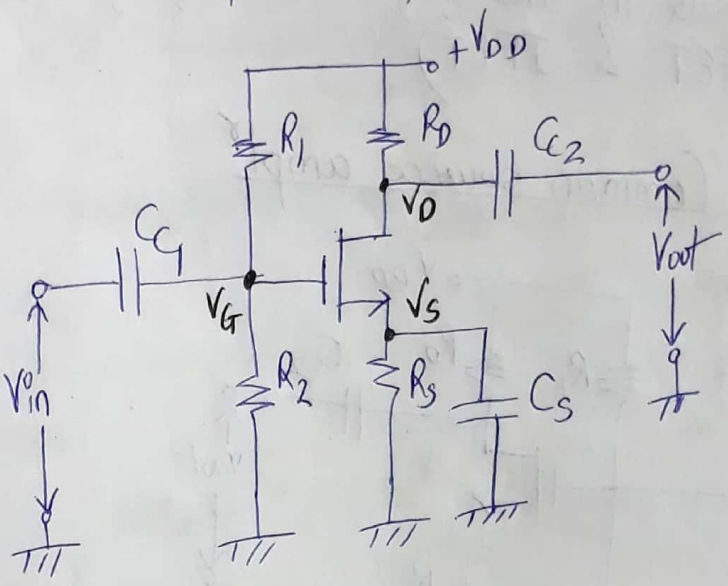
- $A_v = -\dfrac{R_D}{\frac{1}{g_m} + R_S}$
- $Z_i = R_1 \| R_2$
- $Z_o = R_D$

For derivations of A_v, Z_i & Z_o, refer degenerated CS JFET ampl^r analysis

→ Feature of degenerated ampl^r is the reduced voltage gain but a more stable one.

Why -ve sign in Av for CS ampl^r (MOSFET)? 12

Consider CS ampl^r ckt,



$$A_v = -g_m R_D$$

small-sig voltage gain

let say V_{in} ↑ses (Note V_{in} rides on V_G) ie if V_{in} ↑ses, V_G ↑ses
(AC) (DC)

V_S does not change, since C_S blocks DC
(DC)

ie V_G ↑ses, V_S – constant ⇒ $V_{GS} = (V_G - V_S)$ ↑ses

Now, $I_D = K_n(V_{GS} - V_T)^2$ ie if V_{GS} ↑ses → I_D ↑ses

Also, $V_D = V_{DD} - I_D R_D$ ie if I_D ↑ses → V_D ↓ses
ie (V_{out} ↓ses)

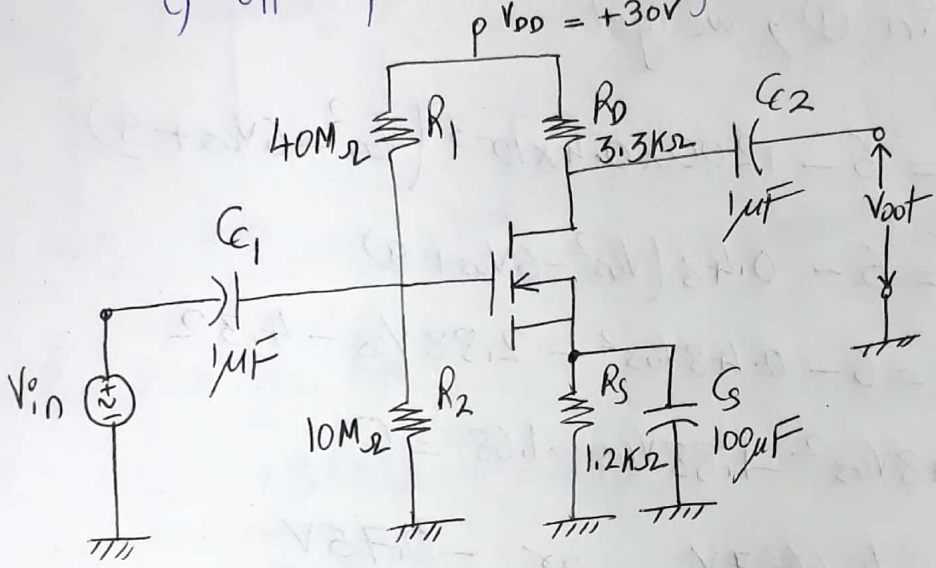
In summary, As V_{in} ↑ses → V_G ↑ses → V_S remain constant

V_{out} ↓ses ← V_D ↓ses ← I_D ↑ses ← V_{GS} ↑ses

Thus, I/P & o/p are out of phase with each other, hence the -ve sign in gain formula

Numerical 01:

Find a) Small-sig voltage gain Av
b) I/p impedance Zi
c) o/p impedance Zo for the circuit below



$V_{GS(th)} = 3V$
$K_n = 0.4 \frac{mA}{V^2}$

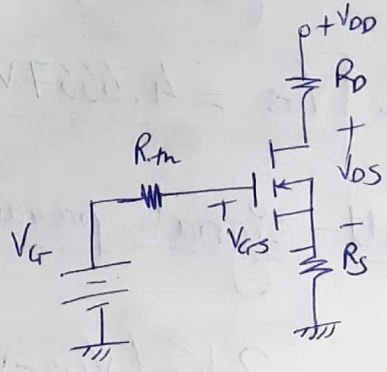
Soln: 1) Above circuit is NMOS-E type CS amplifier

2) **DC Analysis:**

$$V_G = \frac{R_2}{R_1+R_2} \times V_{DD}$$

$$= \frac{10M}{40M+10M} \times 30$$

$$V_G = 6V$$



Now, $V_{GS} = V_G - V_S = 6 - I_D R_S = 6 - I_D(1200) \quad -(1)$

Assuming the given NMOS-E is in saturation region,

$V_T = V_{GS(th)}$

$$I_D = K_n (V_{GS} - V_T)^2 = 0.4m (V_{GS} - 3)^2 \quad \text{— (2)}$$

Put (2) in (1), we get

$$V_{GS} = 6 - 1200 \times 0.4 \times 10^{-3} (V_{GS}^2 - 6V_{GS} + 9)$$

$$V_{GS} = 6 - 0.48 (V_{GS}^2 - 6V_{GS} + 9)$$

$$\text{i.e } V_{GS} = 6 - 0.48 V_{GS}^2 + 2.88 V_{GS} - 4.32$$

$$\text{i.e } 0.48 V_{GS}^2 - 1.88 V_{GS} - 1.68 = 0$$

$V_{GS} = 4.6667V$ or $-0.75V$ ✗

(As $V_{GS} > V_T$)

$\therefore$ $\boxed{V_{GS} = 4.6667V}$

3) Small-signal parameter

r_d or r_o – not given

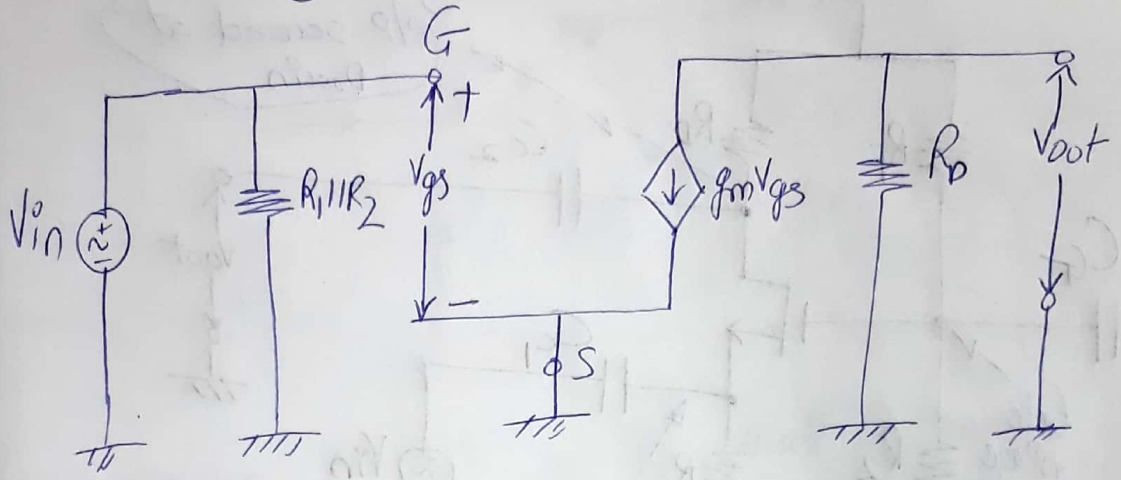
So, assume $\boxed{r_o = \infty}$

$$g_m = 2K_n (V_{GS} - V_T)$$

$$= 2 \times 0.4m (4.6667 - 3)$$

$$\boxed{g_m = 1.3333 \frac{mA}{V}}$$

4) Small-s/g AC analysis:-



a) $A_v = -g_m R_D$

$= -1.3333m \times 3.3K\Omega$

$\boxed{A_v = -4.399}$ --- small-s/g voltage gain

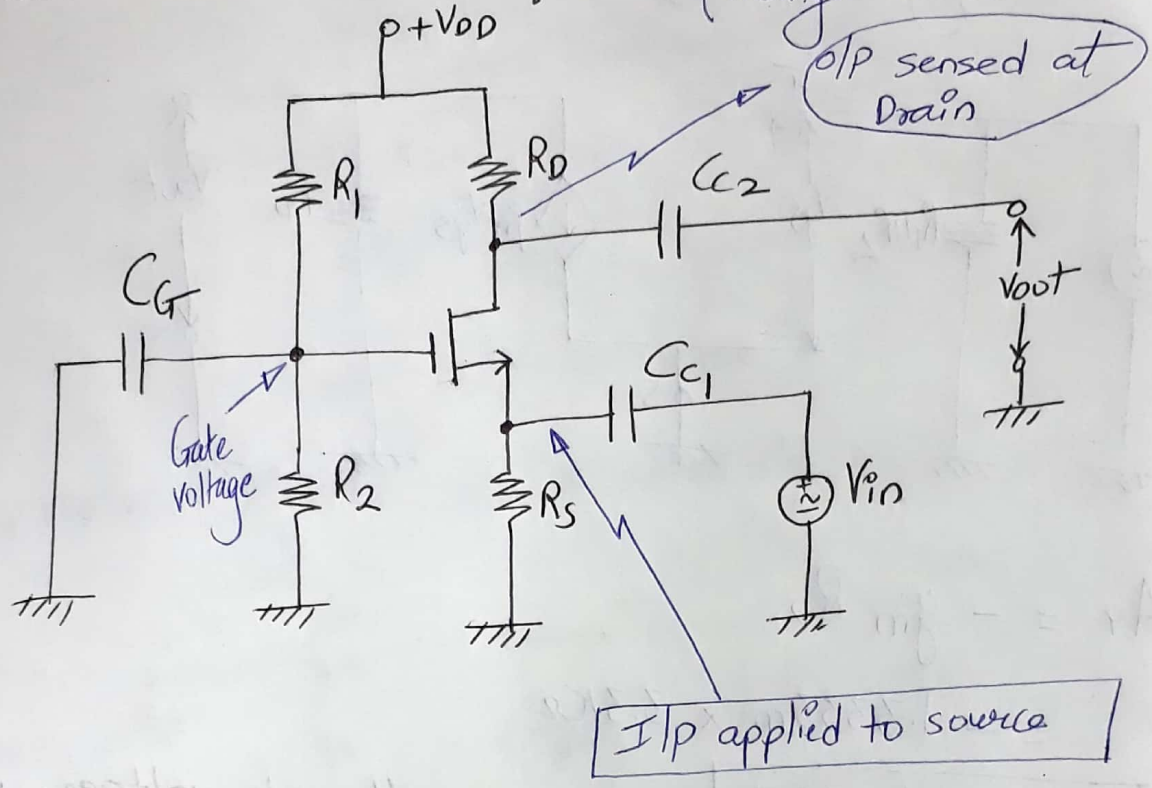
b) $Z_i^o = R_1 \| R_2 = (40M) \| (10M)$

$\boxed{Z_i^o = 8M\Omega}$ --- I/P impedance

c) $Z_o = R_D$

$\boxed{Z_o = 3.3K\Omega}$ ---- O/P impedance

2] Common Gate amplifier : (using NMOS-E device)



Why in CG amplifier, there is no phase difference betn I/p & o/p ?

As Vin ↑ses (Note Vin rides on Vs i.e if Vin ↑ses → Vs ↑ses)
(AC) (DC)

↓
Vs ↑ses ; Now VG = constant (as CG blocks DC)

i.e VGS = (VG - Vs) will ↓se

Also, $I_D = K_n (V_{GS} - V_T)^2$ i.e as VGS ↓ses → ID ↓se

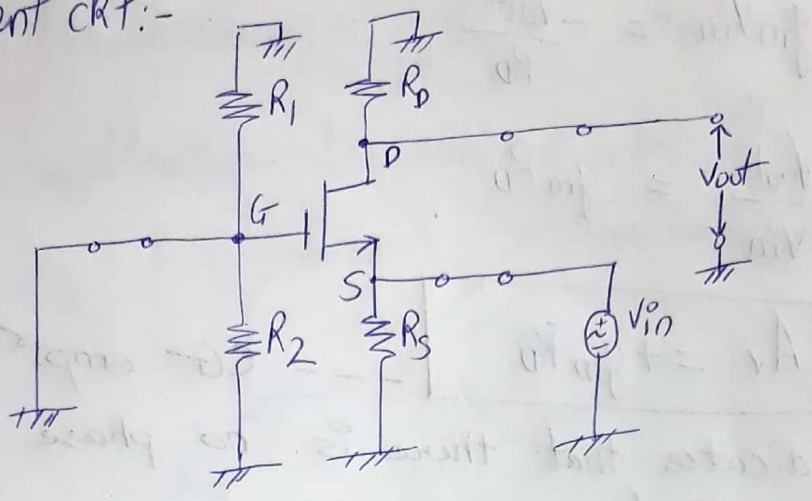
Now, $V_O = V_{DD} - I_D R_D$ i.e as ID ↓ses → VO ↑ses
i.e Vout ↑ses

In summary,

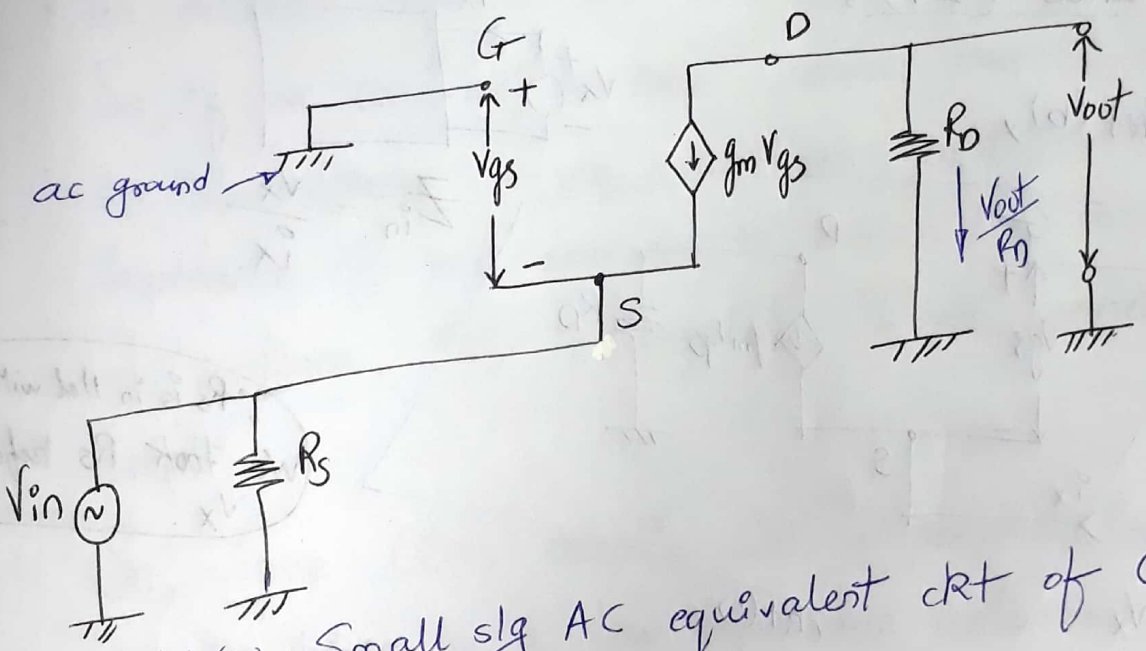
as Vin ↑ses → Vs ↑ses → VG constant i.e VGS ↓ses
↓
Vout ↑ses ← VO ↑ses ← ID ↓ses

This happens → in Common Gate amplifier

AC equivalent ckt:-



Now, replace MOSFET by its small-sig model



ckt(b): Small sig AC equivalent ckt of CG amplr

Analysis:-

a) Small-signal Voltage gain (Av):

From ckt (b), $V_{in} = -V_{gs}$

Applying KCL at 'D' node,

$$g_m V_{gs} + \frac{V_{out}}{R_D} = 0$$

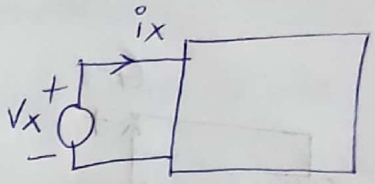
ie $-g_m V_{in} = -\frac{V_{out}}{R_D}$

ie $\frac{V_{out}}{V_{in}} = g_m R_D$

ie $\boxed{A_v = +g_m R_D}$ ---- CG ampl^r

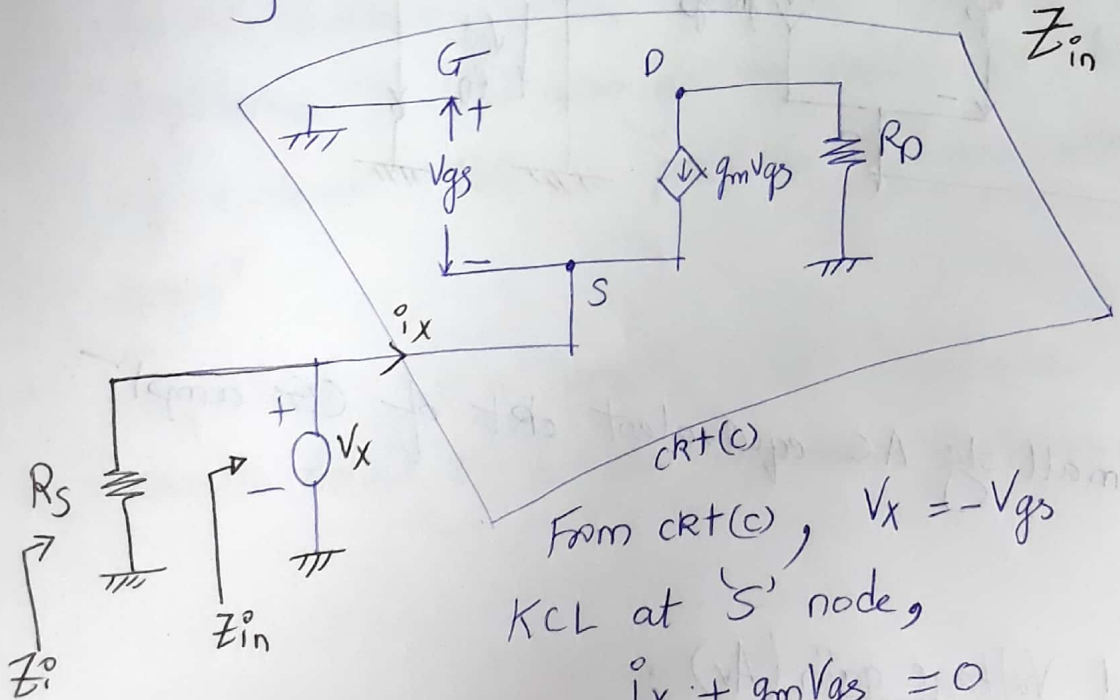
+ve sign indicates that there is no phase difference betn i/p & o/p signals

b) I/p impedance (Z_i) :-



$Z_{in} = \frac{V_x}{i_x}$

Redrawing ckt (b),



ckt (c)

∵ R_S is in ||el with V_x We took R_S before V_x

From ckt (c), $V_x = -V_{gs}$

KCL at 'S' node,

$i_x + g_m V_{gs} = 0$

ie $i_x = g_m V_x$

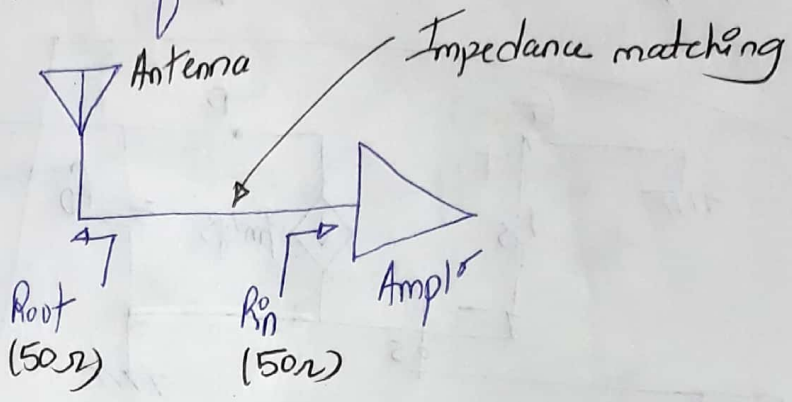
$\frac{V_x}{i_x} = \frac{1}{g_m} \Rightarrow \boxed{Z_{in} = \frac{1}{g_m}}$

$\boxed{Z_i = R_S \,||\, \frac{1}{g_m}}$ → Low value for CG ampl^r

As Z_i (I/P impedance) $= \left(\frac{1}{g_m} \| R_s\right)$ is a low value

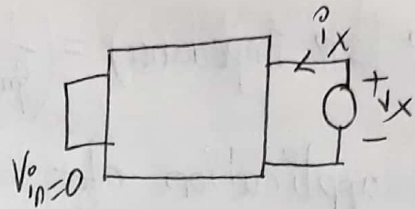
Is there a application of such a ckt ?

Yes



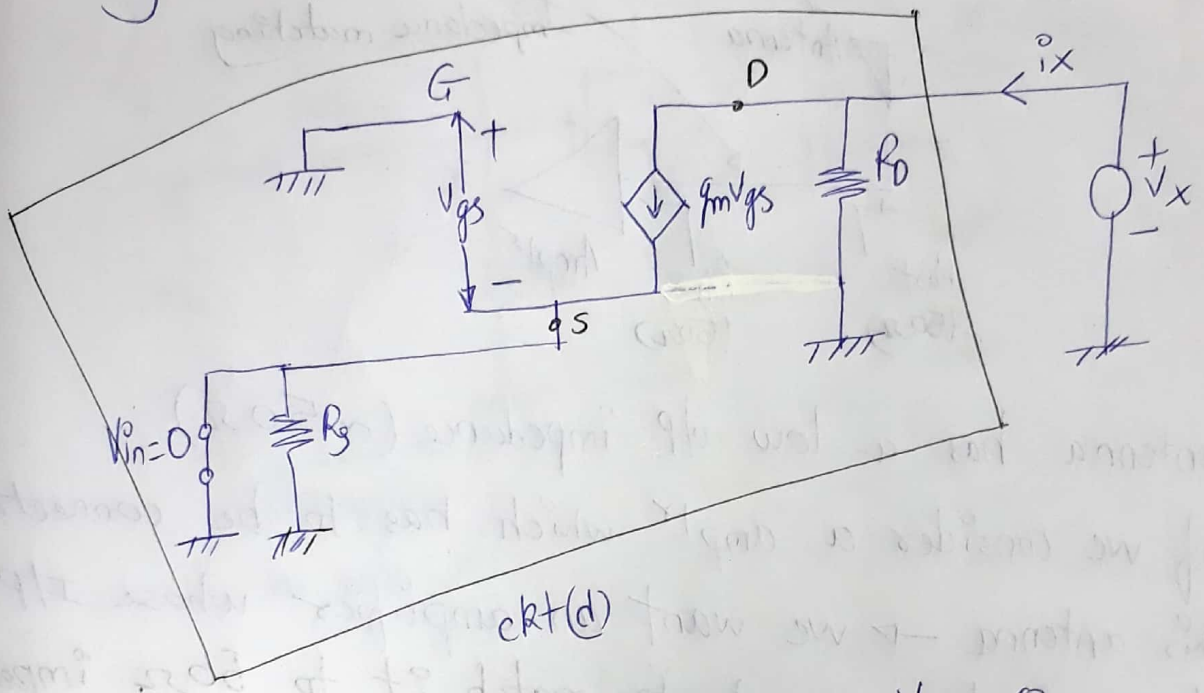
- An antenna has a low o/p impedance (~50Ω)
So, if we consider a ampl^r which has to be connected to this antenna → we want an amplifier whose I/P impedance is low enough to match it to 50Ω impedance of antenna. This is possible if we connect a CG ampl^r.
So, since CG's ampl^{r}s I/P impedance is low → it can be driven by a low impedance antenna.

c) o/p impedance:- Z_o



$$Z_o = \frac{V_x}{i_x}$$

Re-drawing ckt(b),

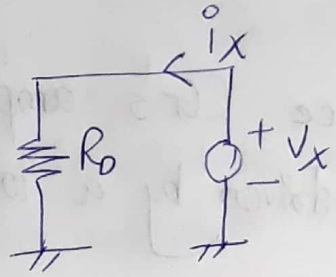


ckt(d)

- In ckt(d), since $V_{in}=0$ ie $V_{gs}=0$

ie ($g_m V_{gs}$) current source is zero ie it has to be a open-ckt.

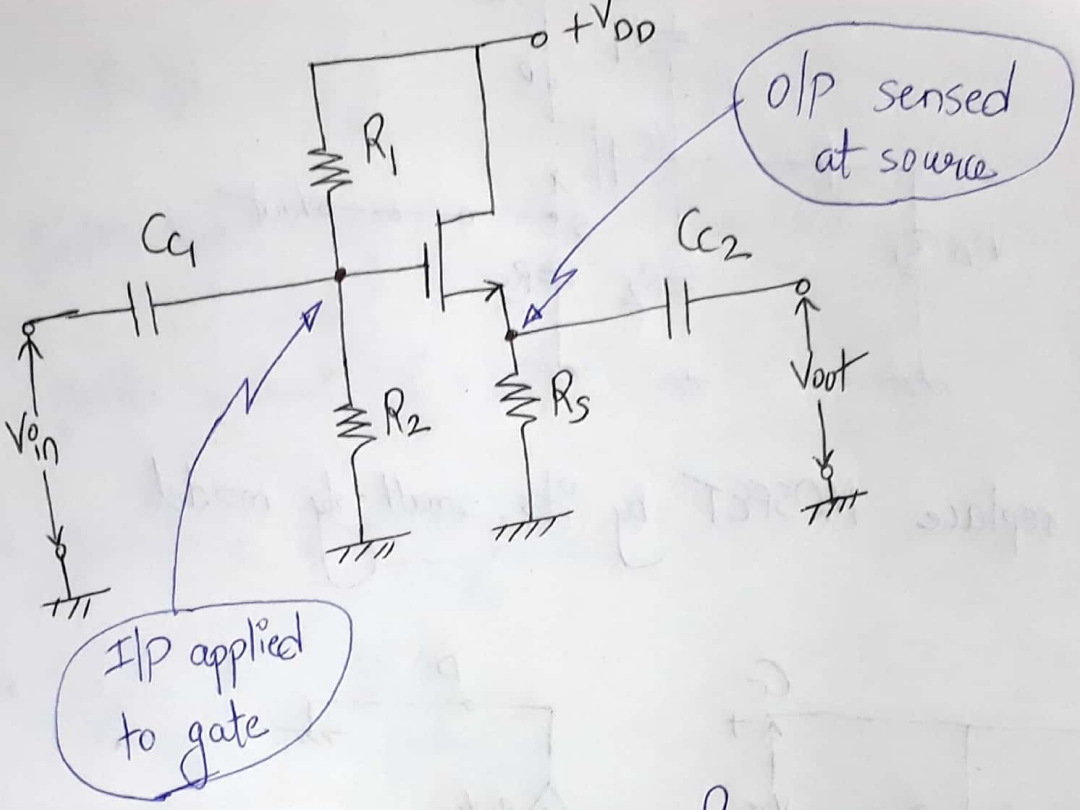
- ckt(d) reduces to



$$\frac{V_x}{i_x} = R_D$$

$$\boxed{Z_o = R_D}$$ --- o/p impedance of CG amplr

3] Common Drain amplifier (Source follower)



Why the name Source follower ?

As V_{in} ↑ses (Note V_{in} rides on V_G ie If V_{in} ↑ses → V_G ↑ses)
(AC) (DC)

→ o/p is at Source, so V_S (ie V_{out}) can { go up / go down / remain same }

$I_D = K_n (V_{GS} - V_T)^2$

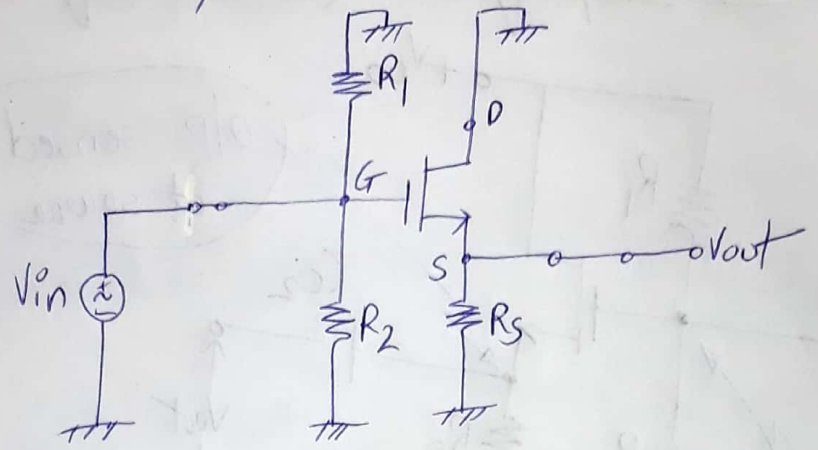
→ let's assume V_S remain same ie $V_S = I_D R_S$ shld be constant
ie I_D must be a constant ⟶ This contradicts that V_G ↑ses

→ Also, V_S cannot go down, as V_{GS} will be a constant then, which again contradicts that V_G ↑ses., V_S ↓ses & I_D remains constant

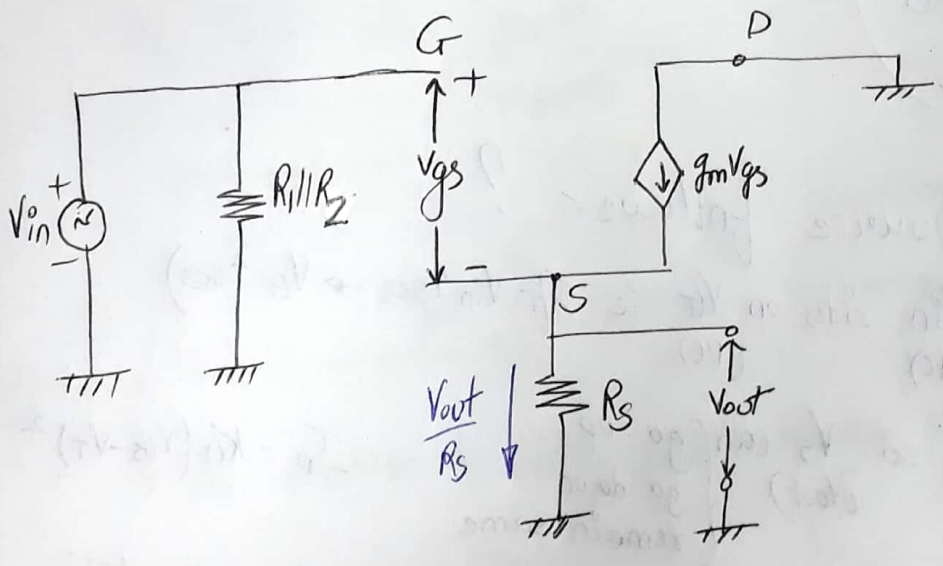
→ Only option left is that V_S to go up ie V_{out} ↑ses as V_{in} ↑ses
ie Source voltage follows the voltage at the gate

Hence, the name "Source follower"

AC equivalent ckt,



Next, replace MOSFET by its small-sig model



ckt(1): Small sig AC equivalent ckt for CD amplifier

Analysis:-

a) Small-signal voltage gain (Av):

Refer ckt (1)

KVL around G-S loop, $V_{in} - V_{gs} - V_{out} = 0$

$V_{gs} = V_{in} - V_{out}$ — (1)

KCL at 'S' node,

$$g_m V_{gs} = \frac{V_{out}}{R_S}$$

$$g_m(V_{in} - V_{out}) = \frac{V_{out}}{R_S} \qquad \text{(From (1))}$$

ie $$g_m V_{in} = V_{out}\left(\frac{1}{R_S} + g_m\right)$$

ie $$g_m V_{in} = V_{out}\frac{(1 + g_m R_S)}{R_S}$$

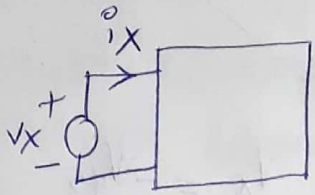
ie $$\frac{V_{out}}{V_{in}} = \frac{g_m R_S}{1 + g_m R_S}$$

$$\boxed{A_v = \frac{R_S}{\frac{1}{g_m} + R_S}}$$ ---- Small-sig voltage gain

---- CD ampl'r

↳ A_v v. close to unity, but always slightly less than 1

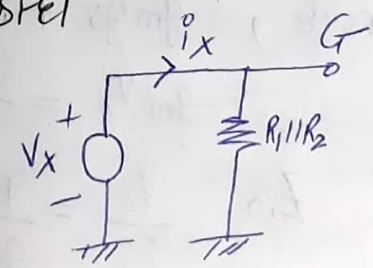
b) I/p impedance (Z_i)



$$Z_i = \frac{V_x}{i_x}$$

In ckt(1), gate to source terminal is open; since $I_G \approx 0$ for MOSFET

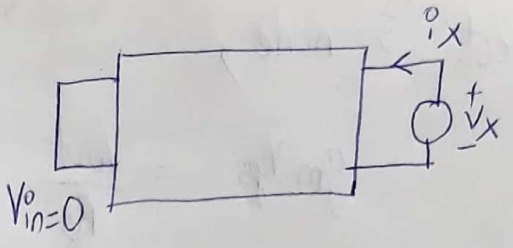
∴ ckt(1) reduces to

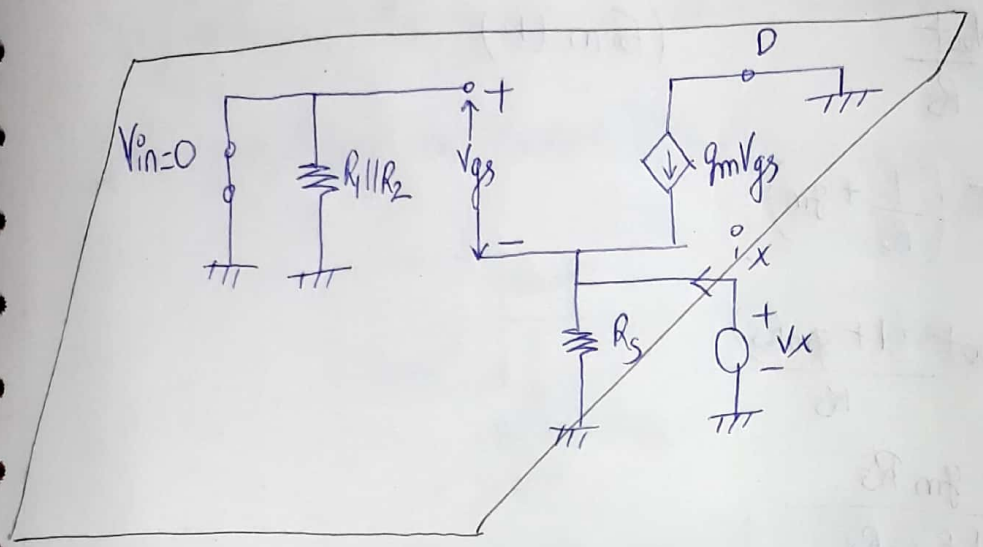


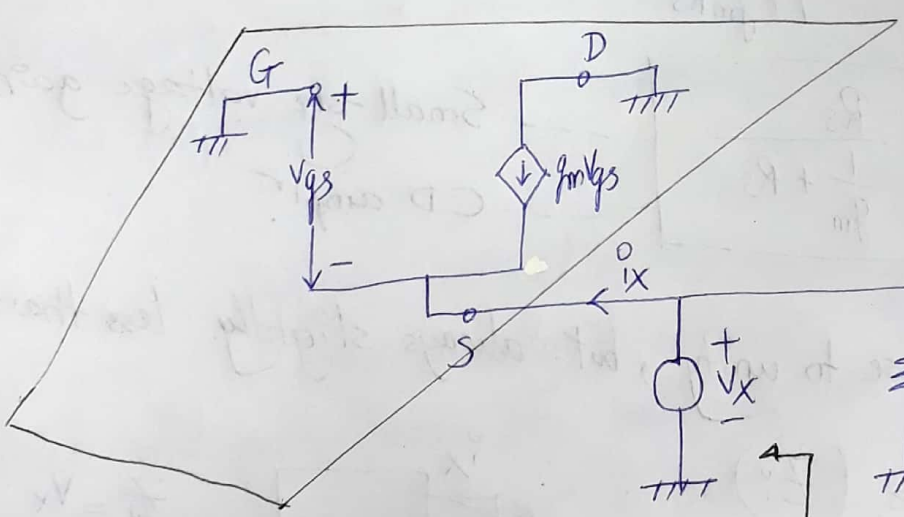
$$\frac{V_x}{i_x} = R_1 \| R_2$$

$$\boxed{Z_i = R_1 \| R_2}$$

c) O/P impedance (Z_o):







we just interchanged V_x & R_S position, to simplify our analysis

ckt (2)

Z_{in}

Z_i

From ckt(2), $V_x = -V_{gs}$

KCL at 'S' node, $g_m V_{gs} + i_x = 0$

$-g_m V_x = -i_x$

$Z_{in} \quad \frac{V_x}{i_x} = \frac{1}{g_m}$

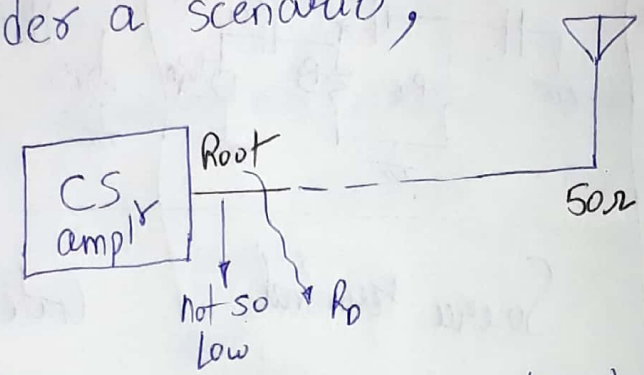
$$\boxed{Z_i = \frac{1}{g_m} \| R_S}$$ Low value of O/P impedance

Where do we use a Source follower ckt?

- The voltage gain Av of source follower is less than 1

So, where is such a ckt useful?

Let's consider a scenario,



let say, we need to connect o/p of CS stage to an antenna.

What happens!

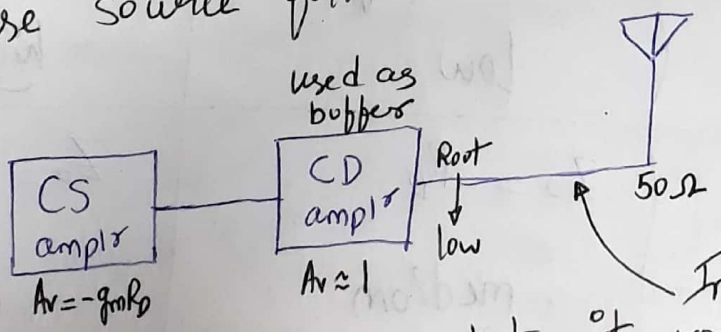
o/p impedance Root $\approx R_D$ (CS stage)

$A_{v_{CS\ stage}} = -g_m R_D$

After connecting o/p of CS stage directly to antenna $A_v = -g_m(R_D \| 50\Omega)$

→ which will poll down the gain of the system.

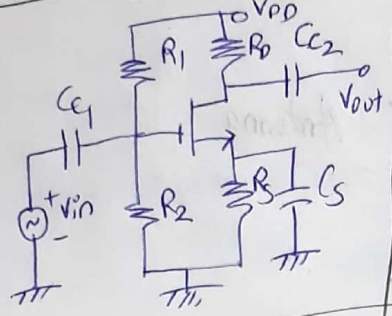
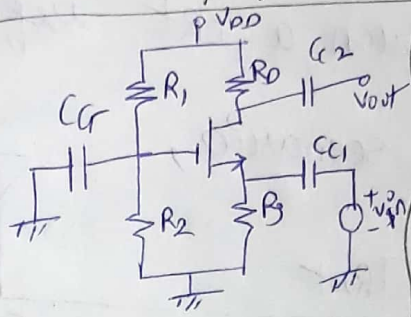
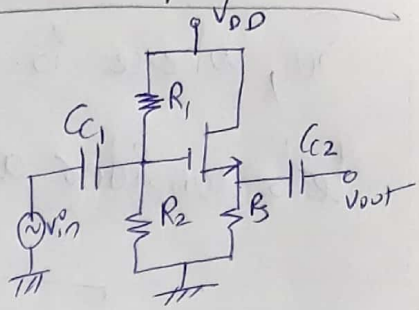
Soln:- Use source follower in betn CS stage & antenna



By connecting source follower ckt, it won't disturb the gain of the system. Also o/p impedance of source follower is low which can easily match the antenna's 50Ω impedance. (ensuring no loss of s/g)

Hence, source follower ckt act as a buffer in this scenario.

Summary of CS, CG & CD amplifiers:-

	Common source amplifier	Common Gate amplifier	Common Drain amplifier
① Circuit			
② I/P sig applied to	Gate terminal	Source terminal	Gate terminal
③ O/P sig measured at	Drain terminal	Drain terminal	Source terminal.
④ Voltage gain	$\boxed{A_v = -g_m R_D}$ → O/P sig out of phase with I/P sig high	$\boxed{A_v = g_m R_D}$ → O/P sig in phase with I/P sig high	$\boxed{A_v = \frac{R_S}{\frac{1}{g_m} + R_S}}$ → O/P & I/P sig in phase Low ($A_v \leq 1$)
⑤ I/P impedance	$Z_i = R_1 \| R_2$ high	$Z_i = R_S \| \frac{1}{g_m}$ Low	$Z_i = R_1 \| R_2$ high
⑥ O/P impedance	$Z_o = R_D$ medium	$Z_o = R_D$ medium	$Z_o = R_S \| \frac{1}{g_m}$ low
⑦ Application	1) can be used as inverting amplifier	1) can be used as an non-inverting amplifier 2) can be driven by low impedance antenna	1) can be used as a voltage buffer. 2) can be used to drive low impedance antenna or speaker

22/11/19

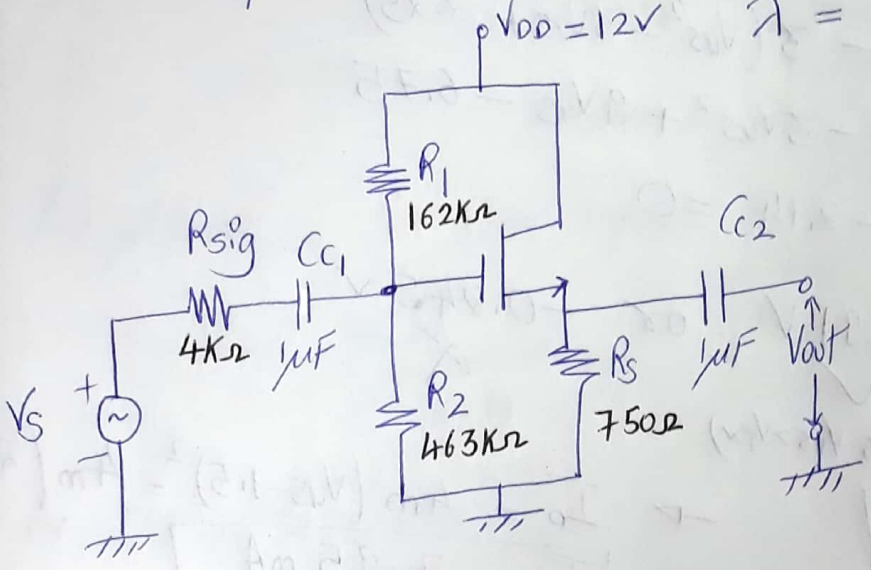
Numerical 02:

Calculate 1) Small-s/g voltage gain

2) Input impedance

3) O/p impedance

Transistor parameters are: $V_{TN} = 1.5\,V$, $k_n = 4\,mA/V^2$, $\lambda = 0.01\,V^{-1}$

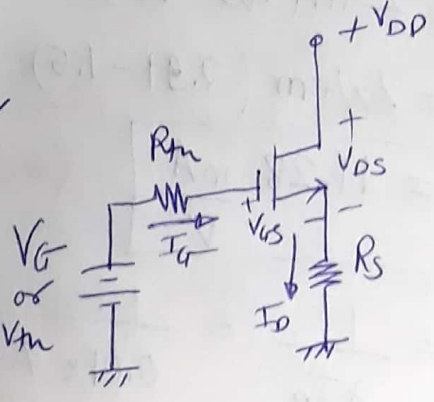


Solution:-

1) Above circuit is NMOS source-follower or common-drain amplifier

2) DC Analysis:-

- $V_G = \frac{R_2}{R_1+R_2} \times V_{DD} = \underline{8.89\ V}$
- $V_{GS} = V_G - I_D R_S$
- $V_{GS} = 8.89 - I_D(750)$ — (1)



KVL to G-S loop,

$V_G - I_G R_{Th} - V_{GS} - I_D R_S = 0$

$I_G = 0$ for MOSFET

$V_{GS} = V_G - I_D R_S$

Assuming given NMOS is working in saturation region,

$$I_D = K_n (V_{GS} - V_{TN})^2$$

$$I_D = 4m (V_{GS} - 1.5)^2 \quad -(2)$$

Put (2) in (1), we get

$$V_{GS} = 8.89 - 750 \times 4m (V_{GS} - 1.5)^2$$

$$V_{GS} = 8.89 - 3 (V_{GS}^2 - 3V_{GS} + 2.25)$$

$$V_{GS} = 8.89 - 3V_{GS}^2 + 9V_{GS} - 6.75$$

$$3V_{GS}^2 - 8V_{GS} - 2.14 = 0$$

$V_{GS} = 2.91\,V$ ✓ or $-0.245\,V$ ✗

(As $V_{GS} > V_{TN}$)

$\therefore$ $\boxed{V_{GS} = 2.91V}$ $\rightarrow$ $I_D = 4m (V_{GS} - 1.5)^2 = 4m (2.91 - 1.5)^2$

$\boxed{I_D = 7.95\,mA}$

3) Small-sig parameters:-

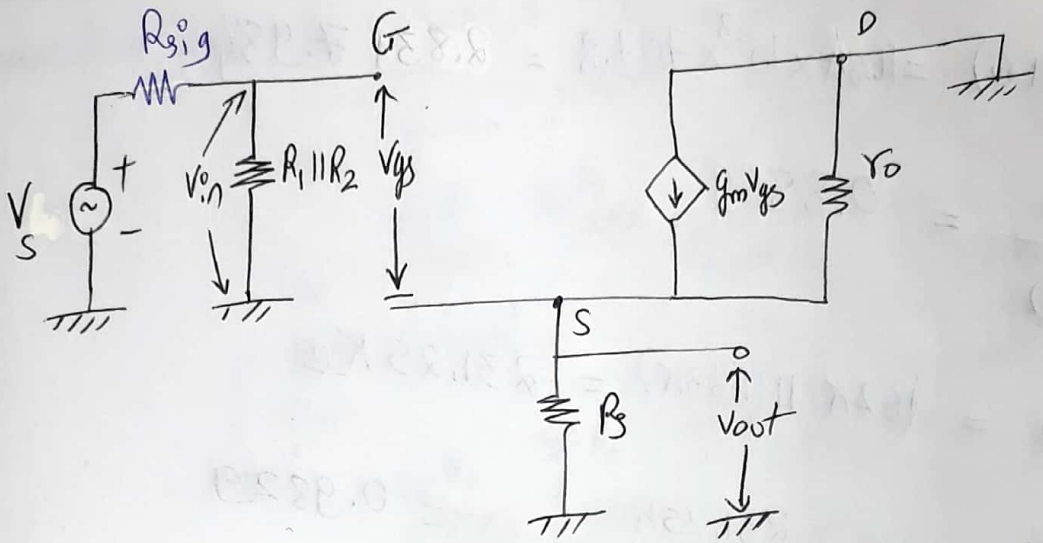
a) $g_m = 2K_n (V_{GS} - V_{TN})$

$= 2 \times 4m (2.91 - 1.5)$

$\boxed{g_m = 11.28\ \frac{mA}{V}}$

b) $r_o = \frac{1}{\lambda I_D} = \frac{1}{0.01 \times 7.95mA} = 12.578\,K\Omega$

Small-signal equivalent circuit,



Av without r_o is given by, (Source-follower)

$$A_v = \frac{g_m R_s}{1 + g_m R_s}$$

$$\boxed{A_v = \frac{V_{out}}{V_{in}}}$$

Av with r_o is given by,

$$A_v = \frac{g_m (R_s \| r_o)}{1 + g_m (R_s \| r_o)}$$

$$A_{vs} = \frac{V_{out}}{V_s} = \frac{V_{out}}{V_{in}} \times \frac{V_{in}}{V_s}$$

$$A_{vs} = A_v \times \frac{V_{in}}{V_s}$$

Now, A_{vs} (Small-sig voltage gain) including R_{sig} is,

$$\boxed{A_{vs} = \frac{g_m (R_s \| r_o)}{1 + g_m (R_s \| r_o)} \times \left(\frac{(R_1 \| R_2)}{R_1 \| R_2 + R_{sig}} \right)}$$

$$V_{in} = \frac{R_1 \| R_2}{R_1 \| R_2 + R_{sig}} V_s$$

Now, we calculate A_{vs} step by step

$R_S \| r_o = 750 \| (12.58K) = \frac{750 \times 12.58K}{750 + 12.58K} = 707.8$

$g_m (R_S \| r_o) = 11.28 \times 10^{-3} \times 707.8 = 7.984$

$\frac{g_m (R_S \| r_o)}{1 + g_m (R_S \| r_o)} = 0.8869$

→ $R_1 \| R_2 = (62K) \| (463K) = 231.25\,K\Omega$

→ $\frac{R_1 \| R_2}{R_1 \| R_2 + R_S} = \frac{231.25K}{231.25K + 4K} = 0.9829$

$A_{VS} = 0.8869 \times 0.9829$

$\boxed{A_{VS} = +0.871}$ --- small-signal voltage gain

→ I/p impedance :-

$Z_i = R_1 \| R_2 = \boxed{231.25K\Omega}$

→ o/p impedance :-

Z_o without r_o was given by, $Z_o = R_S \| \frac{1}{g_m}$

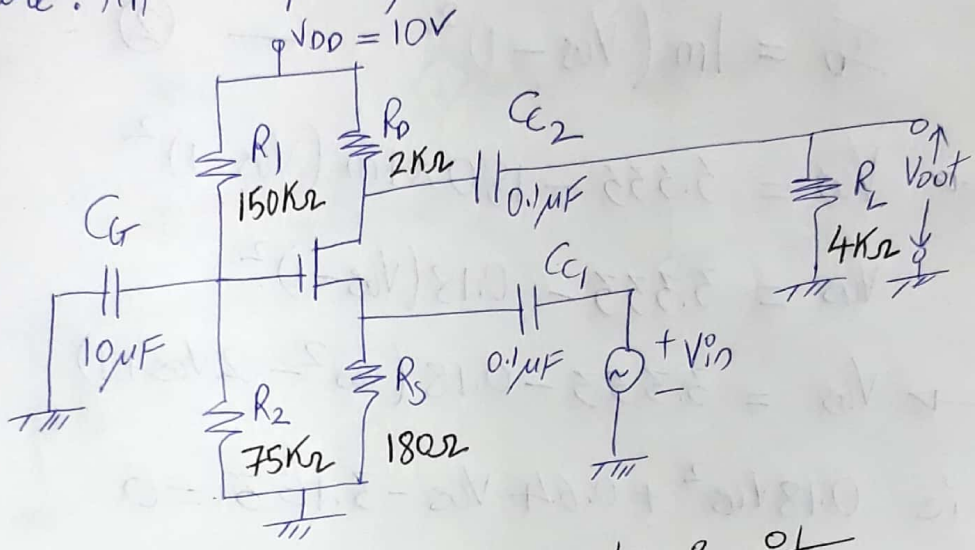
But with r_o, $\boxed{Z_o = R_S \| r_o \| \frac{1}{g_m}}$

$Z_o = 707.8 \| 88.65 = \boxed{78.78\,\Omega}$

One can verify this, using similar analysis as given without r_o

Numerical 03:

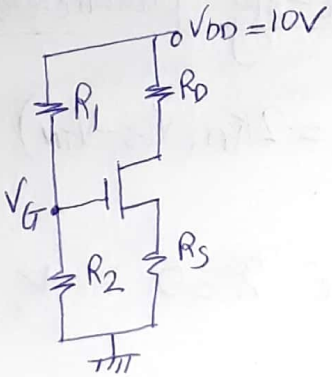
Consider the circuit shown below. The transistor parameters are: $K_n = 1mA/V^2$, $V_{TN} = 1V$, $\lambda = 0$



(1) Draw the small-signal equivalent circuit
(2) Determine the small-signal voltage gain $A_v = \frac{V_{out}}{V_{in}}$
(3) Find the input impedance
(4) Find the o/p impedance

Solution:-

1] Above circuit is NMOS Common Gate amplifier



2] DC Analysis:

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} = 3.333V$$

$$V_{GS} = V_G - V_S = V_G - I_D R_S$$

ie $V_{GS} = 3.333 - I_D(180)$ — ①

ie $I_D = K_n (V_{GS} - V_{TN})^2$

$I_D = I_m (V_{GS} - 1)^2$ — ②

→ $V_{GS} = 3.333 - 180 \times I_m (V_{GS} - 1)^2$

$V_{GS} = 3.333 - 0.18 (V_{GS} - 1)^2$

→ $V_{GS} = 3.333 - 0.18 (V_{GS}^2 - 2V_{GS} + 1)$

ie $0.18 V_{GS}^2 + 0.64 V_{GS} - 3.153 = 0$

Solving, we get

$V_{GS} = 2.77V$ ✓ or $-6.32V$ ✗

$(\because V_{GS} > V_{TN})$

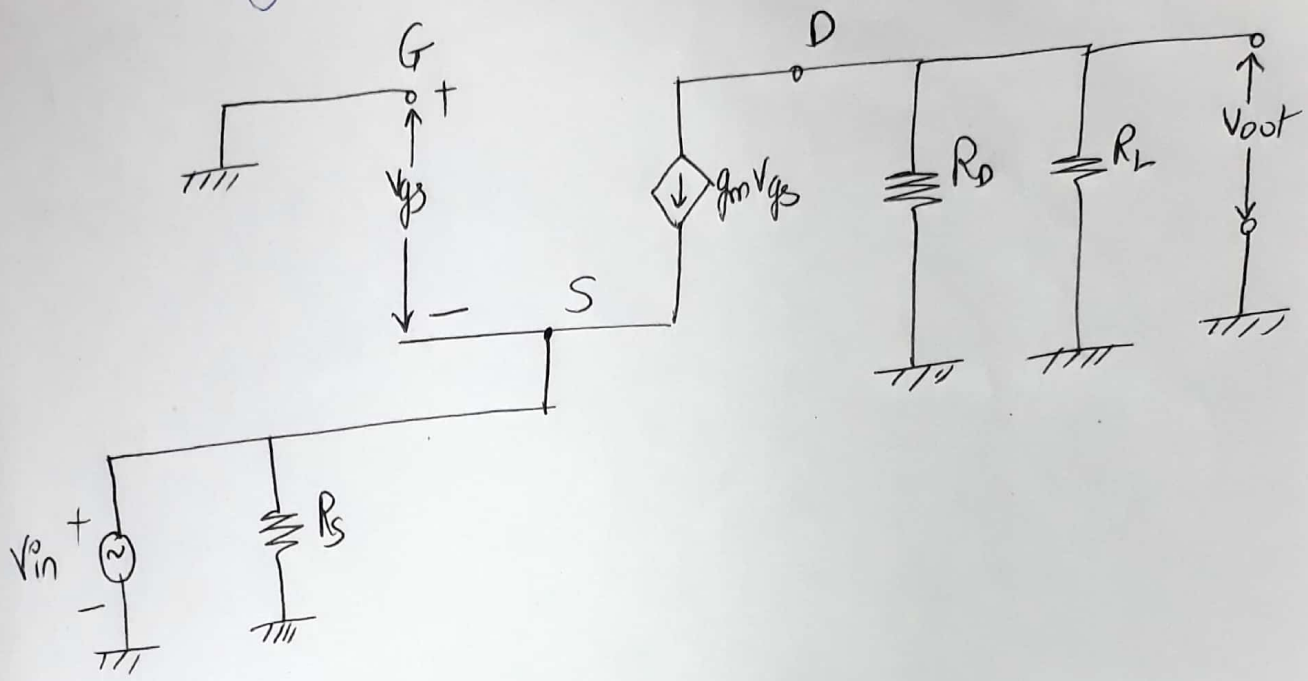
$\boxed{V_{GS} = 2.77V}$ ⟶ $I_D = I_m (2.77 - 1)^2 = \underline{3.13\,mA}$

3] Small-sig parameters :-

$g_m = 2K_n (V_{GS} - V_{TN}) = 3.54 \frac{mA}{V}$

Since $\lambda = 0$ → $r_o = \frac{1}{\lambda I_D} = \underline{\infty}$

4] Small-sig equivalent circuit :



a) Small-signal voltage gain $\left(\frac{V_{out}}{V_{in}}\right)$

$$A_v = g_m (R_D \| R_L)$$

$$= 3.54 \times 10^{-3} (2K \| 4K)$$

$$= 3.54 \times 10^{-3} \times 1.3333K$$

$$\boxed{A_v = 4.72}$$

b) I/p impedance $Z_i = R_S \| \frac{1}{g_m} = 180 \| \frac{1}{3.54 \times 10^{-3}} = 180 \| 282.48$

$$\boxed{Z_i = 109.94}$$

c) o/p impedance $Z_o = R_D \| R_L = 2K \| 4K = 1.33K\Omega$

$$\boxed{Z_o = 1.33K\Omega}$$