MOSFET Characteristics and Parameters:-

MOSFET → Unipolar device

→ Drain o/p current is controlled by an Electric field that depends on a gate control (V_{gs}) voltages.

→ Voltage controlled non-Linear device.

MOSFETs

- Enhancement type MOSFET
  - n-channel MOSFET "NMOS"-E
  - pchannel MOSFET "Pmos"-E
- Depletion-type MOSFET
  - "Nmos"-D
  - "Pmos"-D

- MOSFET's are currently used for VLSI circuits such as microprocessors and memory chips.

- MOSFET differs from the JFET in that (it has gate of the MOSFET is insulated from the channel by a SiO_2 layer), whereas in JFET, gate and channel are separated by a pn junction.

- It is the insulating layer of SiO_2 in the MOSFET construction that accounts for the very desirable high I/P resistance of the device.

$R_i > 10^{10}\,\Omega$

Note: R_i of MOSFET is higher than even JFET

$I_G \approx 0A$ for dc-biased configurations.

1] Depletion-mode MOSFET:-

↳ It has a physical channel between Drain and Source.

a] NMOS-D type:

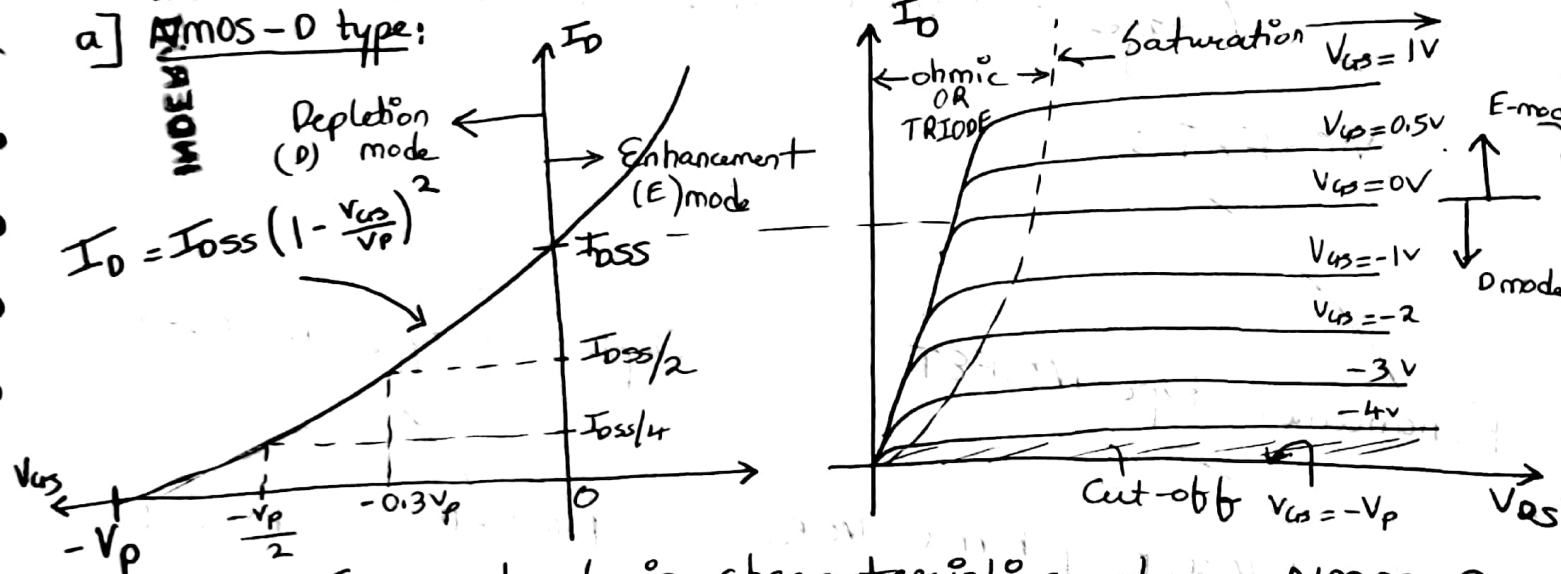

fig 1: Transfer and drain characteristics of an NMOS-D type.

For $V_{GS} = 0 \Rightarrow I_D = I_{DSS}$

For $V_{GS} = -V_P \Rightarrow I_D = 0$

V_P → Pinch-off voltage (similar to one in JFET)

- Primary difference between JFET and D-MOSFET is the fact that depletion-type MOSFETs permits Q-points with possible values of V_{GS} and levels of I_D that exceed I_{DSS} (Refer fig 1 & 2)

b] Pmos - Depletion type:-

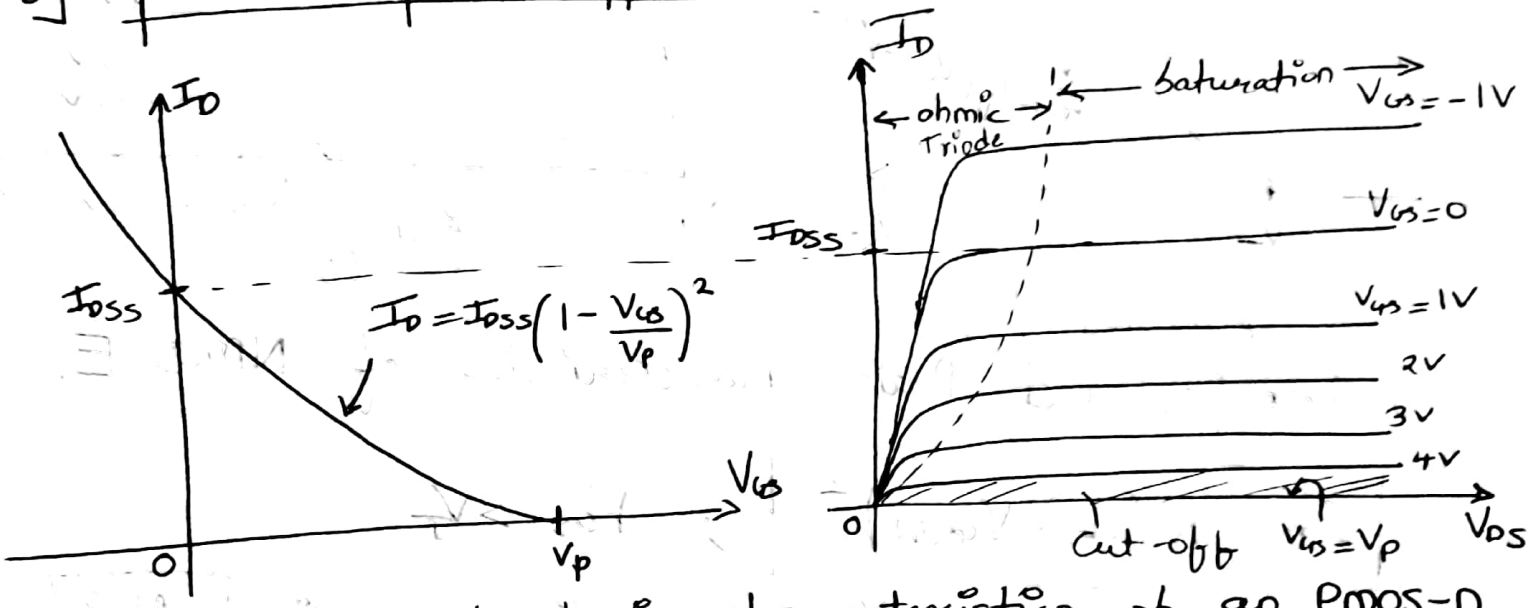

fig2: Transfer and drain characteristics of an Pmos-D type

2] Enhancement-type MOSFET:-

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- It has no physical channel
- operates only in Enhancement-mode and has no depletion mode.

- A channel is induced in an E-MOSFET by the application of a gate-to source voltage $V_{GS} > V_T$.

a] NMOS- Enhancement type:-

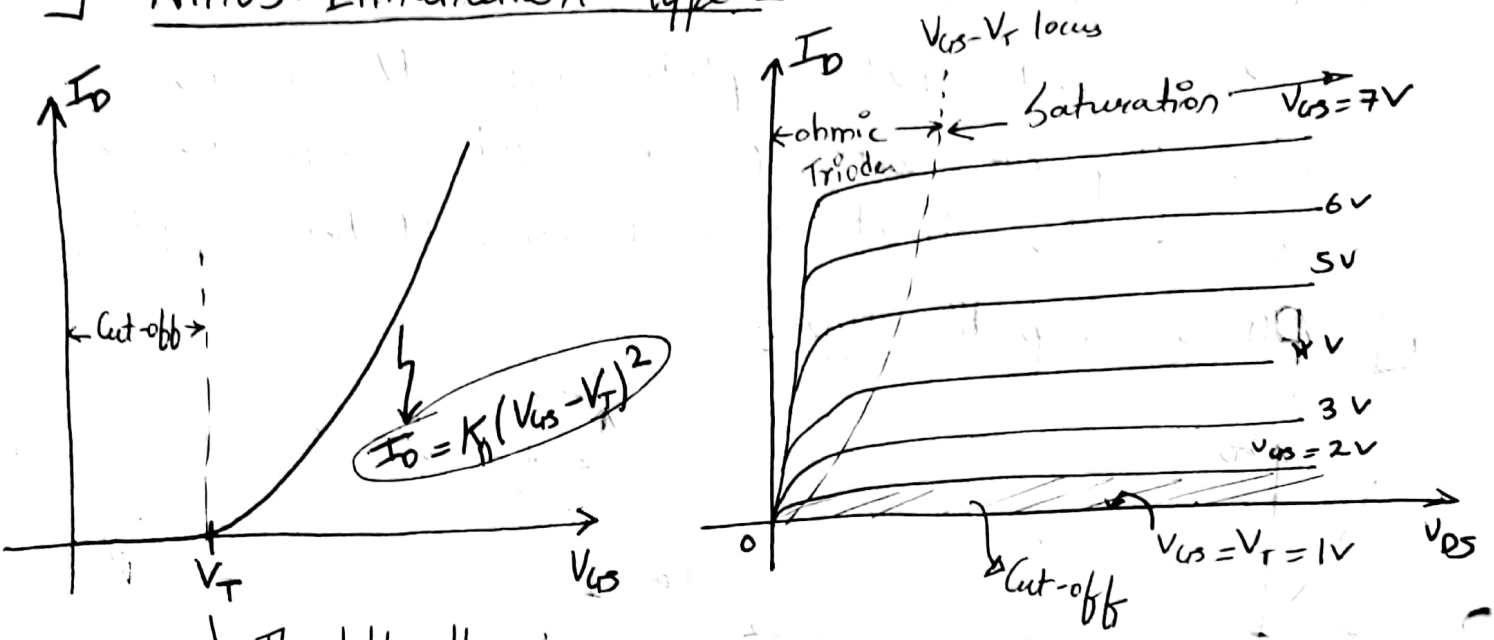


fig 3: Transfer and Drain characteristics of NMOS-E.

$$I_D = K_n(V_{GS} - V_{GS(th)})^2 \quad ; \quad V_{GS} > V_T$$

$$V_{GS(th)} \approx V_t$$

K_n → unit is mA/V^2

. For NMOS-E type, for values of V_{GS} less than V_T, $I_D \approx 0mA$

b] PMOS - Enhancement type:-

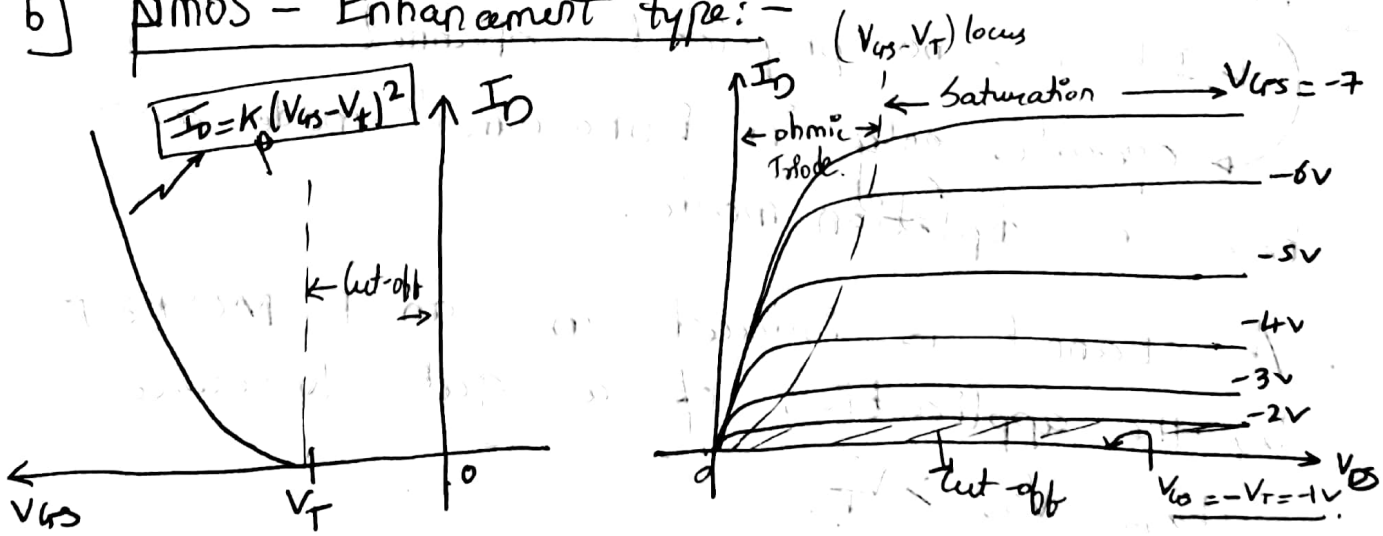
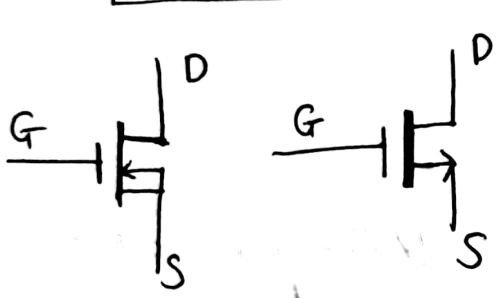


fig 4: Transfer and Drain characteristics of PMOS-E

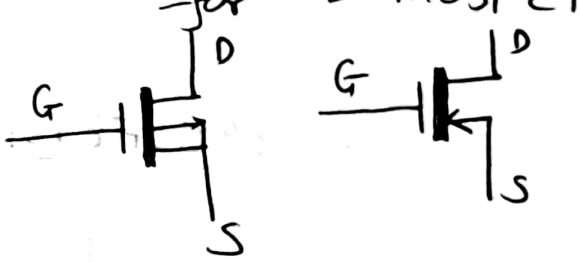
∴ In Enhancement type MOSFETs, there is no drain current when $V_{GS}=0$.

∴ E-MOSFET does not have a I_{DSS} parameter, as do the JFET and D-MOSFET.

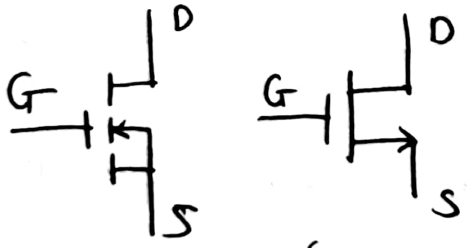
* $\boxed{I_D = K_n(V_{GS}-V_T)^2}$ ---→ Transfer curve expression for E-MOSFET.



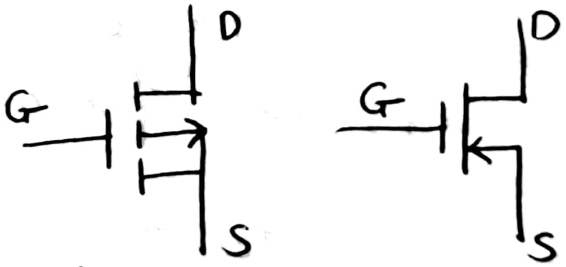
NMOS-D (Symbolic Representations)



PMOS-D



NMOS-E (Symbolic Representations)



PMOS-E

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MOSFET DC Biasing

23/11/19

Biasing → means applying appropriate voltages & current to the device such that it works in the region of operation of interest.

- **Depletion- MOSFET Biasing :-**

  a) Biasing circuits for D-MOSFET are similar to the circuits used for JFET biasing.

  b) The primary difference between the two is that D-MOSFETs can be operated with either +ve or -ve value of V_{GS}

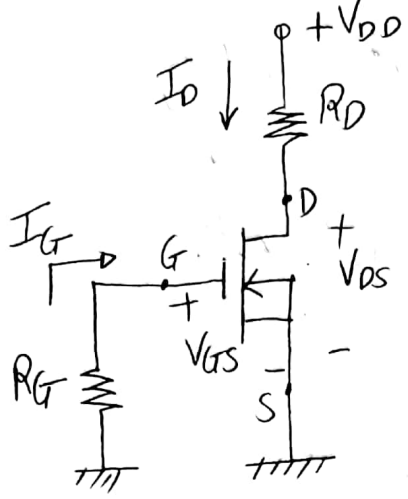
- **D-MOSFET biasing types :-**

  a) Zero-bias

  b) Self-bias

  c) Voltage-divider bias

a) Zero-bias circuit (NMOS-D type):



- Simplest biasing circuit which makes $V_{GS} = 0$

→ KVL to G-S loop,

$$-I_G R_G - V_{GS} = 0$$

But for MOSFET, $I_G \cong 0$ (Because of presence of oxide layer betn Gate & substrate)

ie $\boxed{V_{GS} = 0}$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

For $V_{GS} = 0$; $\boxed{I_D = I_{DSS}}$

→ KVL to D-S loop,

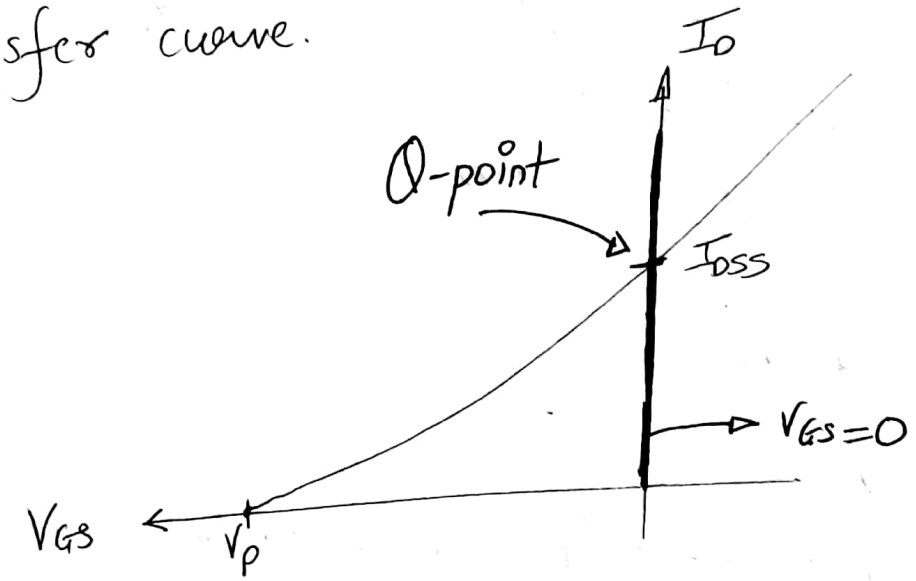
$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$\boxed{V_{DS} = V_{DD} - I_D R_D}$$

To find Q-point graphically :-

Load line is $\boxed{V_{GS} = 0}$

→ Zero-bias circuit will bias NMOS-D at a point lying on the vertical axis of the transfer curve.

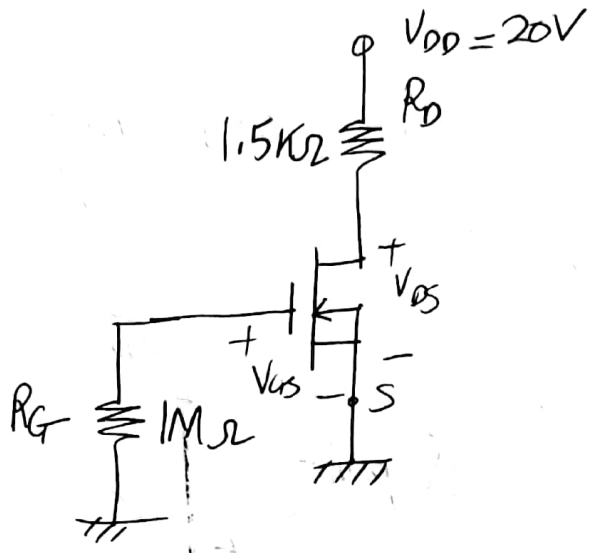


Q-point
$\equiv (V_{GSQ}, I_D)$
$\equiv (0, I_{DSS})$

Note:- Zero-biasing is only possible for depletion-type MOSFETs.

Numerical 01:-

Find the Q-point and V_{DS} for circuit below



$I_{DSS} = 10mA$

$V_P = -4V$.

Soln:- $V_{GS} = V_G - V_S$

From ckt, $V_S = 0$

Also, $V_G = I_G R_G$ ($I_G = 0$ for MOSFET)

$V_G = 0$

i.e $\boxed{V_{GSQ} = 0}$

$$\rightarrow I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(1 - 0\right)^2 = I_{DSS}$$

i.e $I_{DQ} = I_{DSS} = 10\,mA$.

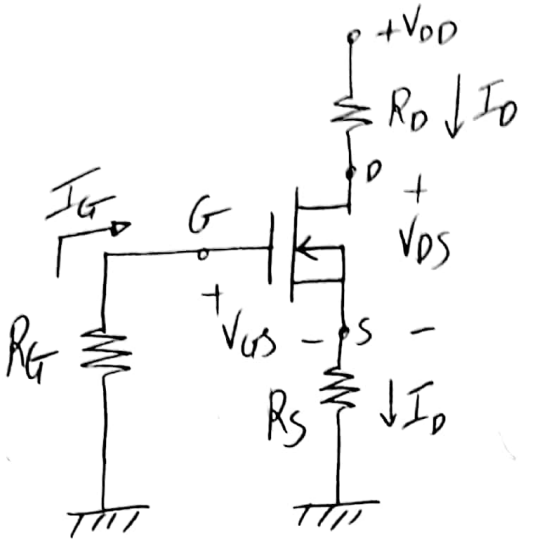
Q point $\equiv (V_{GSQ}, I_{DQ}) \equiv (0, 10\,mA)$

$$\rightarrow V_{DS} = V_{DD} - I_D R_D$$

$$= 20 - 10\,mA \times 1.5K\Omega$$

$$\boxed{V_{DS} = 5V}$$

b) Self-bias circuit (NMOS-D type) :-



$I_D \approx I_S$ for MOSFET

- This biasing ckt gives -ve value of V_{GS}

→ KVL to G-S loop,

$$-I_G R_G - V_{GS} - I_D R_S = 0$$

For MOSFET, $I_G = 0$

$$\boxed{V_{GS} = -I_D R_S}$$

$$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

→ KVL to D-S loop,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\boxed{V_{DS} = V_{DD} - I_D (R_D + R_S)}$$

To determine the Q point graphically :-

For self bias, the eqn of load line is

$$V_{GS} = -I_D R_S \quad -(1)$$

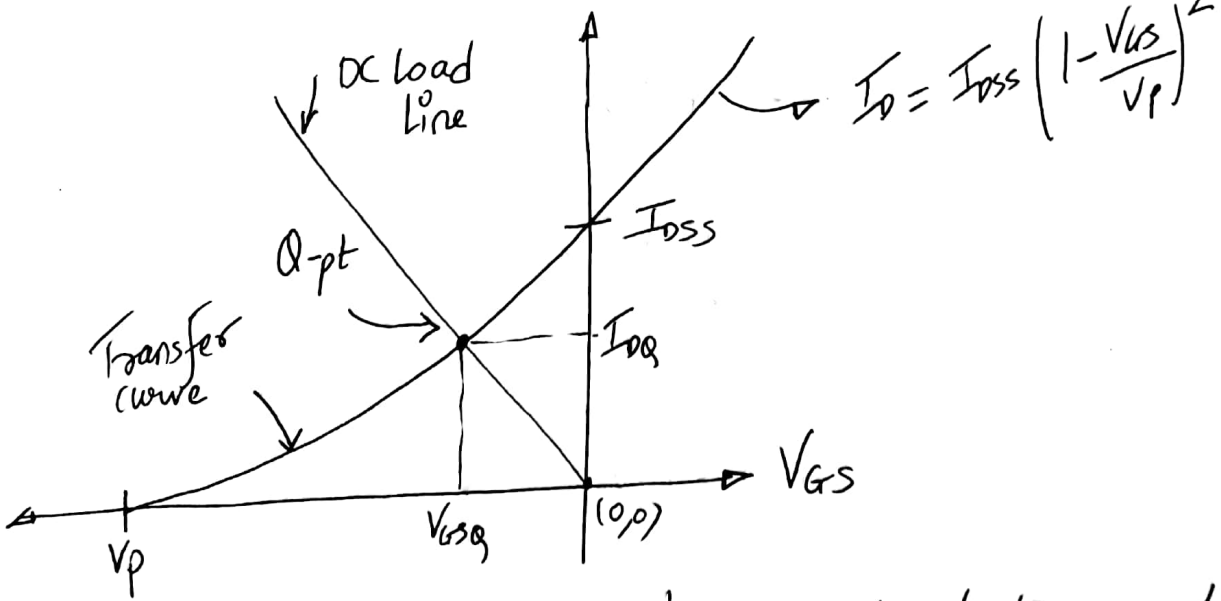
→ Draw transfer curve for NMOS-D type

a) In eqn (1), put $I_D = 0$ → $V_{GS} = 0$

1st point : (0, 0)

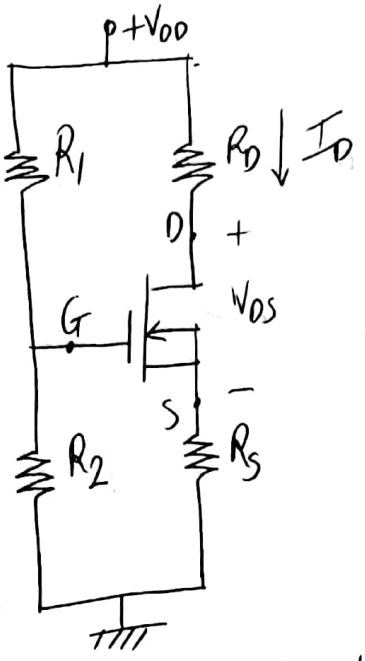
b) In eqn (1), put $I_D = \frac{I_{DSS}}{4}$ → $V_{GS} = -\frac{I_{DSS}}{4} \times R_S$

2nd point : $\left(-\frac{I_{DSS}}{4} \times R_S, \frac{I_{DSS}}{4}\right)$



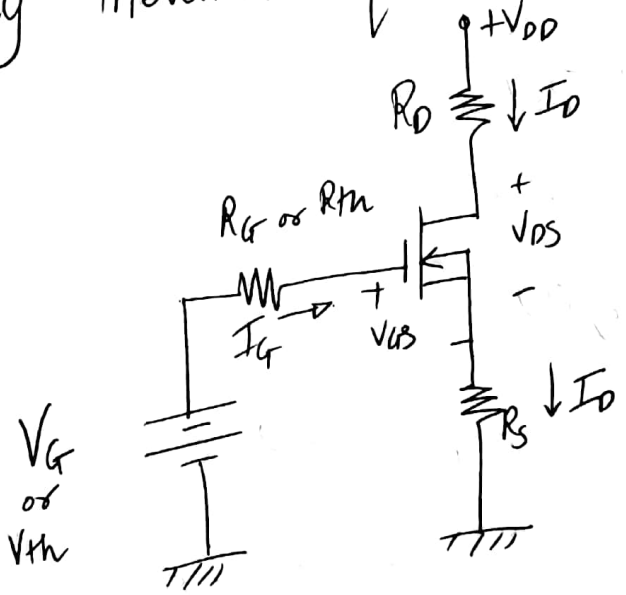
→ Q pt will be the intersection of DC load line and transfer curve.

c) Voltage divider bias (NMOS-D):



- R_1 & R_2 act as voltage divider network

→ Apply thevenin's equivalent to gate, we get



$$V_G = \frac{R_2}{R_1+R_2} \times V_{DD}$$

$$R_G = R_1 \,||\, R_2$$

KVL to G-S loop,

$$V_G - I_G R_G - V_{GS} - I_D R_S = 0$$

But $I_G = 0$ for MOSFET

ie $$\boxed{V_{GS} = V_G - I_D R_S}$$

Also, $$\boxed{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

KVL to D-S loop,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\boxed{V_{DS} = V_{DD} - I_D (R_S + R_D)}$$

- To determine the Q-point graphically :-

$$\boxed{V_{GS} = V_G - I_D R_S}$$ ---- Load line eqn for voltage-divider bias

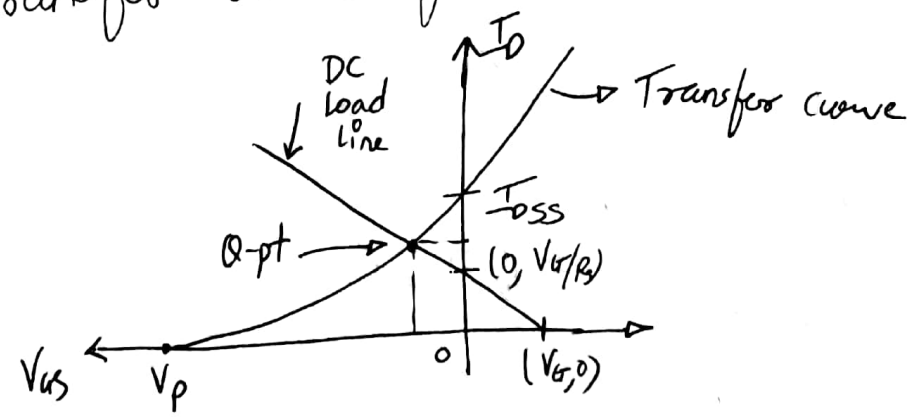
1) Put $V_{GS} = 0 \rightarrow I_D = \frac{V_G}{R_S}$

1st point $\equiv \left(0, \frac{V_G}{R_S}\right)$

2) Put $I_D = 0 \rightarrow V_{GS} = V_G$

2nd point $\equiv (V_G, 0)$

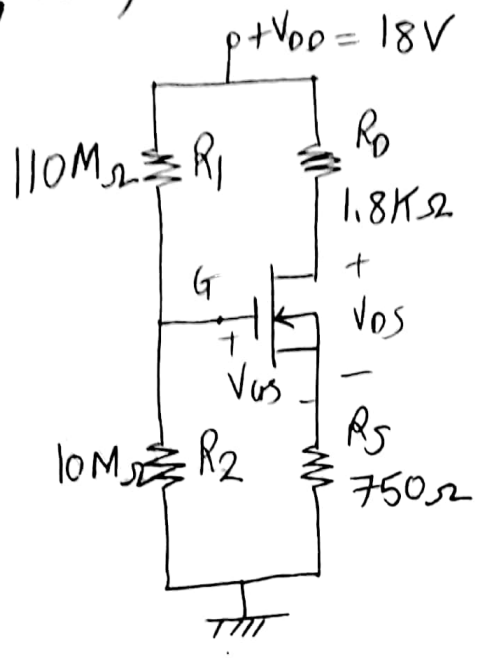
- Draw transfer curve for NMOS-D device



→ Q-point will be the intersection of DC load line and transfer curve

Numerical 02

Find V_G, V_{GS}, I_D and V_{DS} for circuit below:-



$I_{DSS} = 6mA$

$V_P = -3V$

. Above ckt is NMOS-D type voltage-divider bias

Solution: $V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \underline{1.5V}$

$V_S = I_D R_S$

$\rightarrow V_{GS} = V_G - V_S = V_G - I_D(750)$

ie $V_{GS} = 1.5 - I_D(750)$ — (1)

Now, we assume that given NMOS-D device is working in saturation region.

$\therefore I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 6mA\left(1 + \frac{V_{GS}}{3}\right)^2$ — (2)

Put (2) in (1), we get

$V_{GS} = 1.5 - 750 \times 6mA\left(1 + \frac{V_{GS}}{3}\right)^2$

$$V_{GS} = 1.5 - 4.5\left(1 + \frac{2}{3}V_{GS} + \frac{V_{GS}^2}{9}\right)$$

i.e $V_{GS} = 1.5 - 4.5 - 3V_{GS} - 0.5V_{GS}^2$

$\rightarrow 0.5V_{GS}^2 + 4V_{GS} - 3 = 0$

Solving, we get

$V_{GS} = -0.8377V$ or $-7.16V$

(As $V_{GS} > V_P$)

$\rightarrow \boxed{V_{GS} = -0.8377V}$

$\rightarrow I_D = 6mA\left(1 - \frac{(-0.8377)}{(-3)}\right)^2 = 3.11mA$

i.e $\boxed{I_D = 3.11mA}$

KVL to D-S loop,

$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

i.e $V_{DS} = V_{DD} - I_D(R_D + R_S)$

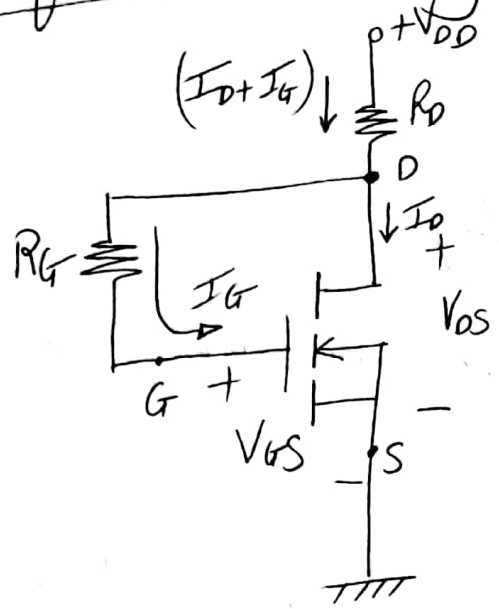
$= 18 - 3.11 \times 10^{-3}(1.8K + 750)$

$\boxed{V_{DS} = 10.07\ V}$

- Enhancement-type NMOS Biasing :-

- E-MOSFET (n-channel) requires V_{GS} value greater than threshold value (V_T)
- So, a self-bias cannot be used since it makes V_{GS} negative.
- Also, a zero-bias cannot be used since it makes V_{GS} zero.
- Types of E-NMOS biasing
  a) Drain feedback bias
  b) Voltage-divider bias
- In NMOS-E type biasing, V_{GS} can only take +ve values (as $V_{GS} > V_T$)

a) Drain-feedback biasing (NMOS-E)



KVL to G-S loop,

$$V_{DD} - (I_D + I_G) R_D - I_G R_G - V_{GS} = 0$$

For MOSFET, $I_G \approx 0$

ie $$V_{DD} - I_D R_D - V_{GS} = 0$$

$$\boxed{V_{GS} = V_{DD} - I_D R_D}$$

For E-type NMOS,

$$\boxed{I_D = K_n (V_{GS} - V_T)^2}$$

→ KVL to D-S loop,

$$V_{DD} - I_D R_D - V_{DS} = 0$$

ie $$\boxed{V_{DS} = V_{DD} - I_D R_D}$$

For Drain-feedback bias, we can write

$$\boxed{V_{DS} = V_{GS} = V_{DD} - I_D R_D}$$

- To determine Q-point graphically.

$$\boxed{V_{GS} = V_{DD} - I_D R_D} \quad \text{---- Load line eq}^n$$

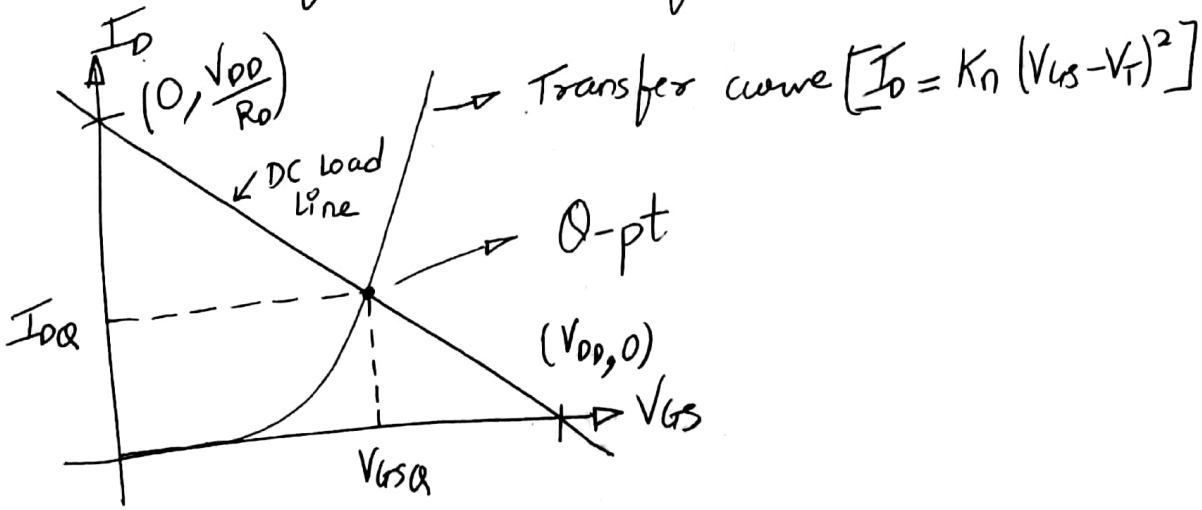
a) Put $V_{GS} = 0 \rightarrow I_D = \frac{V_{DD}}{R_D}$

1^{st} point $\equiv \left(0, \frac{V_{DD}}{R_D}\right)$

b) Put $I_D = 0 \rightarrow V_{GS} = V_{DD}$

2^{nd} point $\equiv (V_{DD}, 0)$

→ Draw transfer curve of NMOS-E :

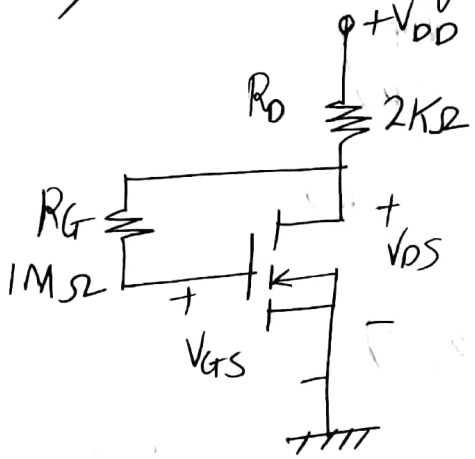


→ Intersection of DC load line & transfer curve gives us the Q-point

Note: Drain feedback bias provides a stable Q-point, because it tends to compensate for any changes in device parameter variations.

Numerical 03:

Find V_{GS}, I_D & V_{DS} for the circuit below



$I_{D(on)} = 6mA$

$V_{GS(on)} = 8V$

$V_{GS(th)} = 3V$

Soln:- 1) $K_n = \dfrac{I_{D(on)}}{[V_{GS(on)} - V_{GS(th)}]^2}$

$= \dfrac{6mA}{(8-3)^2}$

$K_n = 0.24 \ \dfrac{mA}{V^2}$

$V_{GS} = V_{DD} - I_D R_D$

ie $V_{GS} = 12 - I_D(2000)$ — (1)

Assume the given NMOS-E is in saturation region,

$I_D = K_n (V_{GS} - V_{GS(th)})^2$

ie $I_D = 0.24 \times 10^{-3} (V_{GS} - 3)^2$ — (2)

Put (2) in (1), we get

$\rightarrow V_{GS} = 12 - 0.48(V_{GS} - 3)^2$

$V_{GS} = 12 - 0.48(V_{GS}^2 - 6V_{GS} + 9)$

ie $V_{GS} = 12 - 0.48V_{GS}^2 + 2.88V_{GS} - 4.32$

ie $0.48V_{GS}^2 - 1.88V_{GS} - 7.68 = 0$

$V_{GS} = 6.41V$ or $V_{GS} = -2.49V$

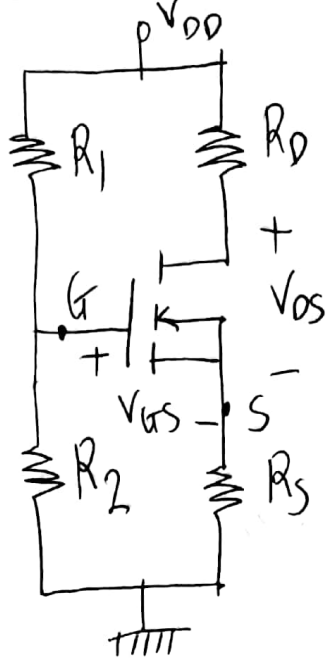
$(V_{GS} > V_{GS(th)})$ ✓ X

ie $\boxed{V_{GS} = 6.41V}$ ie $\boxed{V_{DS} = V_{GS} = 6.41V}$

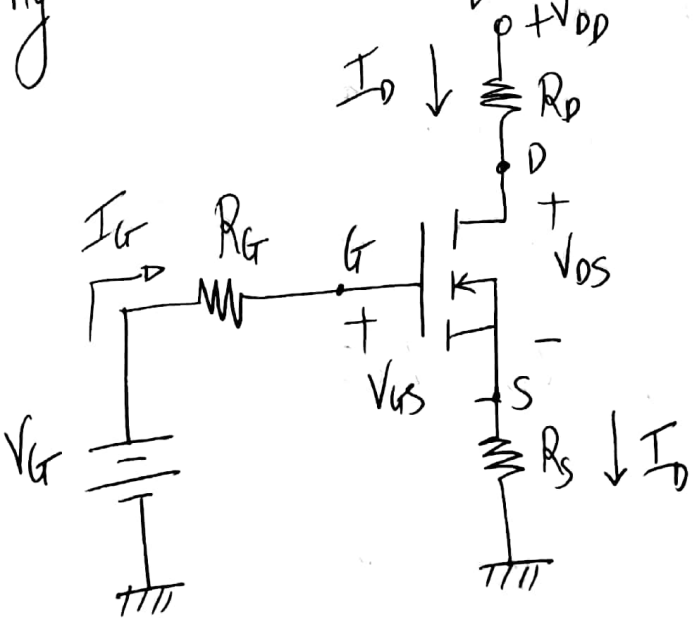
$I_D = K_n(V_{GS} - 3)^2 = 0.24 \times 10^{-3}(6.41 - 3)^2$

$\boxed{I_D = 2.79mA}$

b) Voltage-divider bias (NMOS-E) :-



Applying thevenin's equivalent at the gate terminal,



$$V_G = \frac{R_2}{R_1+R_2} V_{DD}$$

$$R_G = R_1 \| R_2$$

Apply KVL to G-S loop,

$$V_G - I_G R_G - V_{GS} - I_D R_S = 0$$

For MOSFET, $I_G = 0$

$$\boxed{V_{GS} = V_G - I_D R_S}$$

$$\boxed{I_D = K_n (V_{GS} - V_T)^2}$$

KVL to D-S loop,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\boxed{V_{DS} = V_{DD} - I_D (R_D + R_S)}$$

- To determine Q-point graphically :

$$\boxed{V_{GS} = V_G - I_D R_S}$$ — Load Line eqⁿ

① Put $V_{GS} = 0$ $\rightarrow$ $I_D = \frac{V_{DD}}{R_S}$

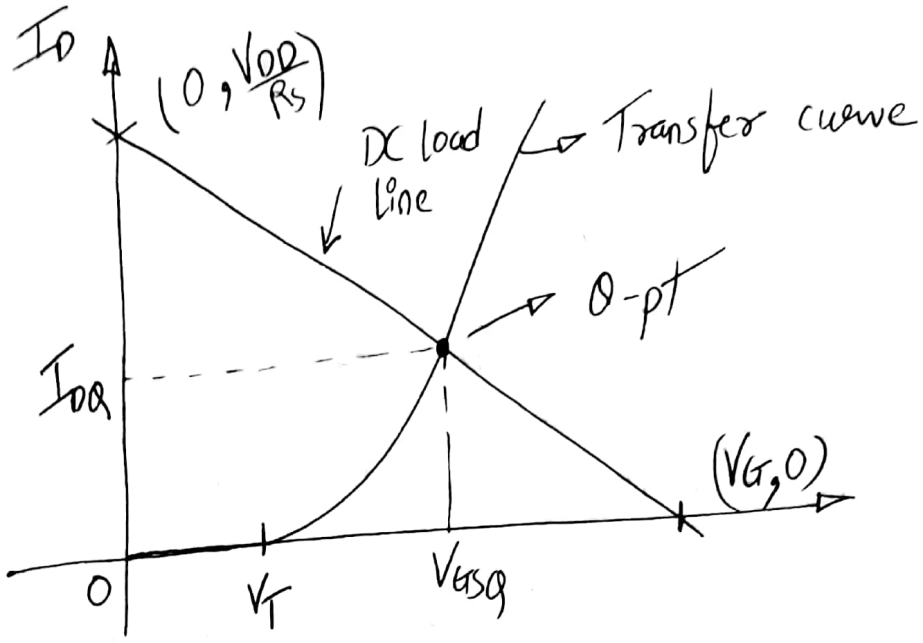
1st point $\equiv \left(0, \frac{V_{DD}}{R_S}\right)$

② Put $I_D = 0$ $\rightarrow$ $V_{GS} = V_G$

2nd point $\equiv (V_G, 0)$

Now, we draw the transfer curve of NMOS-E type device using,

$$\boxed{I_D = K_n (V_{GS} - V_T)^2}$$



→ Q-point is the intersection of DC load line & transfer curve

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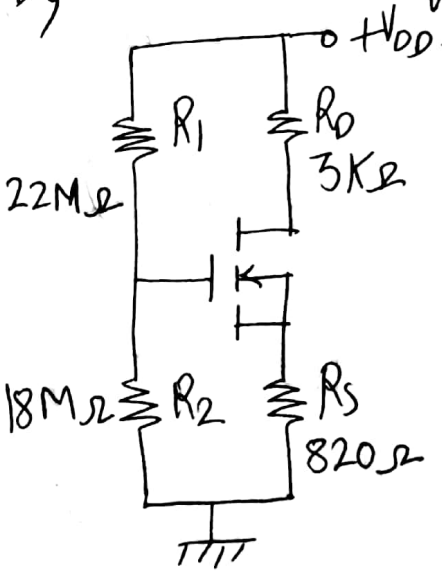
Numerical 04:

Find V_G, I_D, V_{GS} and V_{DS} for circuit shown below

Also, determine region of operation of given device



Given data

$V_{GS(th)} = 5V$
$V_{GS(on)} = 10V$
$I_{D(on)} = 3mA$

Soln:

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{18M}{18M + 22M} \times 40 = 18\,V$$

For E-NMOS transistor,

$$K_n = \frac{I_{D(on)}}{[V_{GS(on)} - V_{GS(th)}]^2}$$

$$= \frac{3mA}{[10-5]^2}$$

$$\boxed{K_n = 0.12 \frac{mA}{V^2}}$$

$$\rightarrow V_{GS} = V_G - V_S = V_G - I_D R_S$$

$$V_{GS} = 18 - I_D(820) \quad -(1)$$

Assuming that given NMOS-E transistor is working in saturation region,

$$I_D = K_n (V_{GS} - V_{GS(th)})^2$$

$$I_D = 0.12 \times 10^{-3} (V_{GS} - 5)^2 \quad -(2)$$

Put (2) in (1), we get

$$V_{GS} = 18 - 820 \times 0.12 \times 10^{-3} (V_{GS} - 5)^2$$

$$V_{GS} = 18 - 0.0984 (V_{GS}^2 - 10V_{GS} + 25)$$

$$V_{GS} = 18 - 0.0984 V_{GS}^2 + 0.984 V_{GS} - 2.46$$

ie $$0.0984 V_{GS}^2 + 0.016 V_{GS} - 15.54 = 0$$

Solving, we get

$V_{GS} = 12.48V$ ✓ or $-12.64V$ ✗

(as $V_{GS} < V_{GS(Th)}$)

$$\therefore \boxed{V_{GS} = 12.48V}$$

ie $$I_D = K_n (V_{GS} - 5)^2$$

$$= 0.12 \times 10^{-3} (12.48 - 5)^2$$

$$\boxed{I_D = 6.72\,mA}$$

Now, $$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

$$= 40 - 6.72\,mA\,(3K + 820)$$

$$\boxed{V_{DS} = 14.32V}$$

$V_{GS(Th)} = V_T$

Since, $[V_{GS} > V_{GS(Th)}]$ & $V_{DS} > V_{GS} - V_T$

$V_{DS} > (12.48 - 5)$

$\therefore$ Given NMOS-E device is working in the saturation region.

Design of MOSFET biasing circuits

Design 01

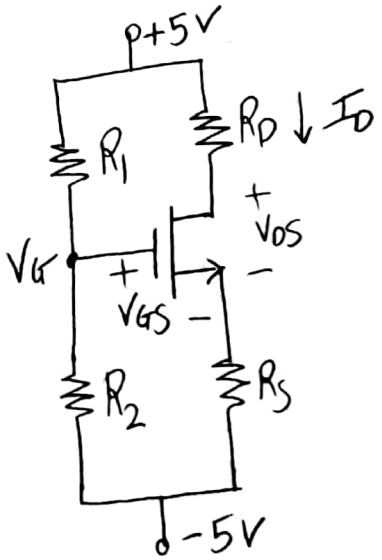
Design a NMOS-E DC Biasing circuit to give

$I_D = 0.25\,mA$, $V_{DSQ} = 4V$, $V_{R_S} = 1V$

MOSFET parameters : $K_n' = 80\mu A/V^2$, $\frac{W}{L} = 4$, $V_{TN} = 1.2V$

The current in the bias resistors (R_1 & R_2) should be approximately $20\mu A$

V_{DD} and V_{SS} = +5V and -5V



Sol^n: $V_{R_S} = R_S I_{DQ}$

$$R_S = \frac{V_{R_S}}{I_{DQ}} = \frac{1V}{0.25\,mA} = 4\,K\Omega$$

Select $\boxed{R_S = 3.9K\Omega\,(std)\,,\ 1/4W}$ (L.S.V)

KVL to D-S loop,

$$V_{DD} - I_{DQ}R_D - V_{DS} - I_{DQ}R_S + V_{SS} = 0$$

$$5 - I_{DQ}(R_D + R_S) - 4 + 5 = 0$$

$\underline{I_{DQ} = 0.25mA}$ --- given & $R_S = \underline{3.9K\Omega}$

$$R_D = 20.1K\Omega$$

Select $\boxed{R_D = 22K\Omega, 1/4W_{(std)}}$ (H.S.V)

$$I_D = K_n (V_{GS} - V_T)^2$$

$$I_D = \frac{K_n'}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

$$0.25mA = \frac{80\mu}{2} \times \cancel{4}^{2} \times (V_{GS} - 1.2)^2$$

$$1.5625 = (V_{GS} - 1.2)^2$$

$$\boxed{V_{GS} = 2.45V}$$

Since, current through bias resistors is 20μA

$$R_1+R_2 = \frac{V_{DD}+V_{SS}}{I_{(R_1+R_2)}} = \frac{5+5}{20\mu A} = 500K\Omega$$

- $V_G = \left[\frac{R_2}{R_1+R_2}(5+5)\right] - 5$
- $V_G = \frac{R_2 \times 10}{500K} - 5$
- $V_S = I_D R_S - 5$

→ $V_{GS} = V_G - V_S$

$$2.45 = \left[\frac{R_2 \times 10}{500K} - 5\right] - [I_D R_S - 5]$$

(R_S = 3.9KΩ, I_D = 0.25mA)

$$2.45 = \frac{R_2}{50K} - 5 - 0.975 + 5$$

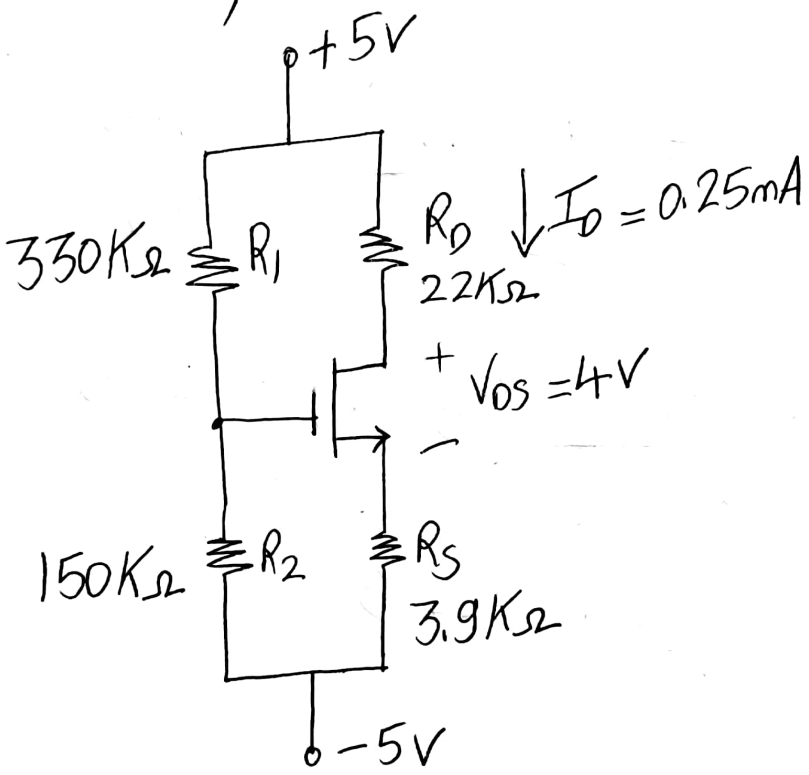
$$3.425 = \frac{R_2}{50K\Omega} \Rightarrow R_2 = 171.25K\Omega$$

Select $R_2 = 150K\Omega$ (std), 1/4W L.S.V

$R_1 = 328.75K\Omega$ (∵ $R_1+R_2 = 500K$)

Select $R_1 = 330K\Omega$ (std), 1/4W H.S.V

Designed circuit,



Design 02:

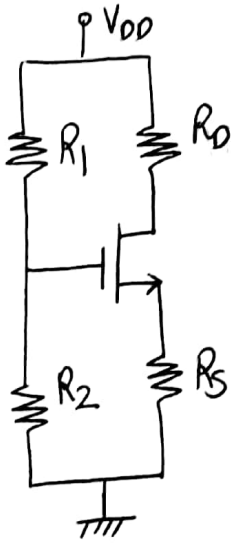
Design an N-channel E-type MOSFET using voltage-divider bias for following specifications:-

$I_{DQ} = 5mA$, $V_{DSQ} = 5V$

MOSFET paramcters: $K_n = 25 \frac{mA}{V^2}$, $V_{TN} = 1V$

Soln:

1) Since we want Qpoint on center of DC load Line, we select $V_{DD} = 2V_{DSQ} = 10V$



2) Assume $V_G = 25\%$ of V_{DD}

$V_G = 0.25 \times 10 = 2.5V$

$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD}$

$$2.5 = \frac{R_2}{R_1 + R_2} \times 10$$

Assume $\boxed{R_2 = 100K\Omega, 1/4W}$

$$2.5 = \frac{100K}{R_1 + 100K} \times 10$$

$$R_1 = 300K\Omega$$

Select $\boxed{R_1 = 330K\Omega, 1/4W \text{ (std)}}$

3) $I_D = K_n (V_{GS} - V_T)^2$

$$5mA = 25mA\ (V_{GS} - 1)^2$$

$$\boxed{V_{GS} = 1.447V}$$

- $V_{GS} = V_G - I_D R_S$

$$1.447 = 2.5 - I_D R_S$$

$$I_D R_S = 1.053$$

$$R_S = \frac{1.053}{5mA} = 210.6\Omega$$

Select $\boxed{R_S = 180\Omega, 1/4W \text{ (std)}}$

4) KVL to D-S loop gives,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$I_D R_D = V_{DD} - V_{DS} - I_D R_S$$

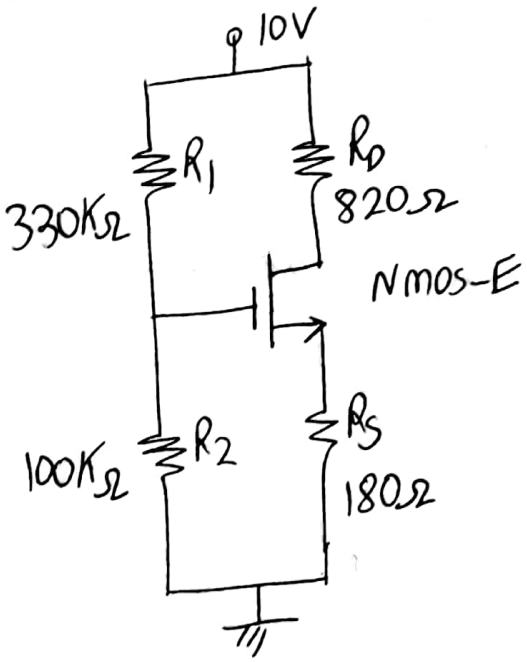
$$R_D = \frac{V_{DD} - V_{DS} - I_D R_S}{I_D}$$

$$= \frac{10 - 5 - 5mA \times 180}{5mA}$$

$$R_D = 820\Omega$$

Select $\boxed{R_D = 820\Omega, 1/4W}$

5) Designed ckt is,

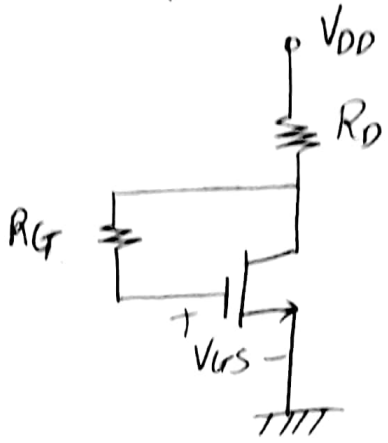


Design 03: Design an NMOS-E drain-feedback bias circuit for following specifications

$V_{DSQ} = 5V$, $I_{DQ} = 5mA$

MOSFET parameters : $K_n = 25 \frac{mA}{V^2}$, $V_{TN} = 1.2V$

Soln: 1) Circuit Diagram



2) Since, we want the Q-point at center of DC load line

$V_{DD} = 2V_{DSQ} = 10V$

3) Selection of R_G :-

To maintain high input impedance & to minimize loading effect , R_G value has to be kept high

Select $\boxed{R_G = 1M\Omega, 1/4W}$ (std)

4) For drain-to feedback bias,

$$V_{DS} = V_{DD} - I_D R_D$$

$$5 = 10 - 5mA \times R_D$$

$$R_D = \frac{5V}{5mA} = 1K\Omega$$

Select $\boxed{R_D = 1.2K\Omega (std),\ 1/4W}$

5) Designed circuit is