Introduction to Multi-gate MOSFETs

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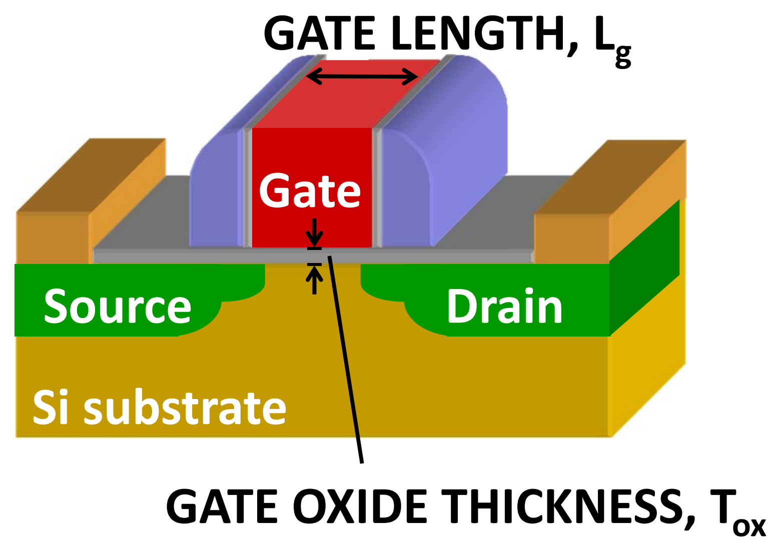
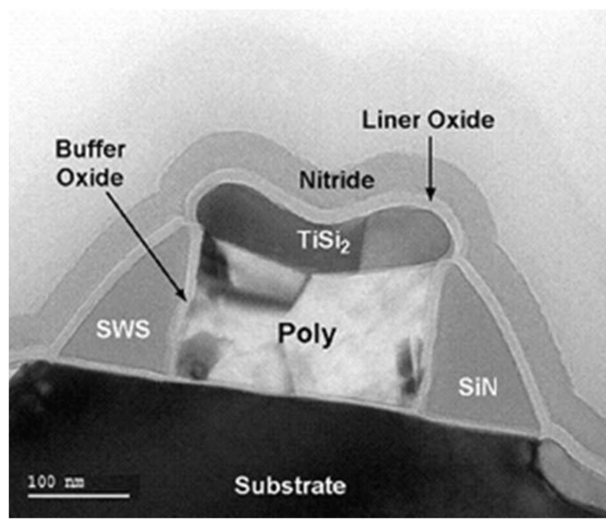
MOSFET Fundamentals

Metal Oxide Semiconductor Field-Effect Transistor:



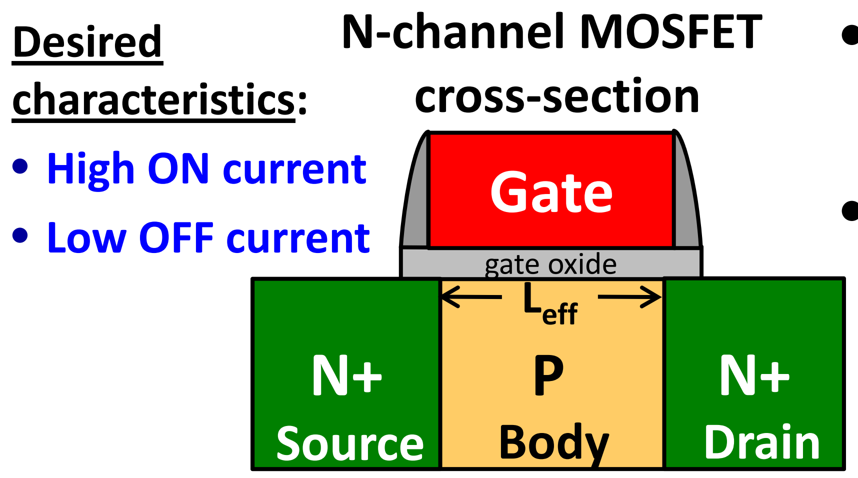
0.25 micron MOSFET XTEM



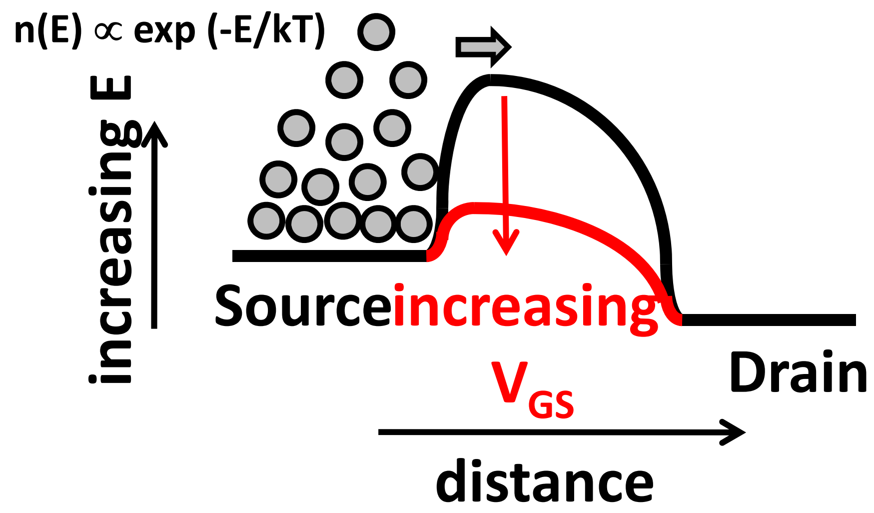
http://www.eetimes.com/design/automotive-design/4003940/LCD-driver-highly-integrated

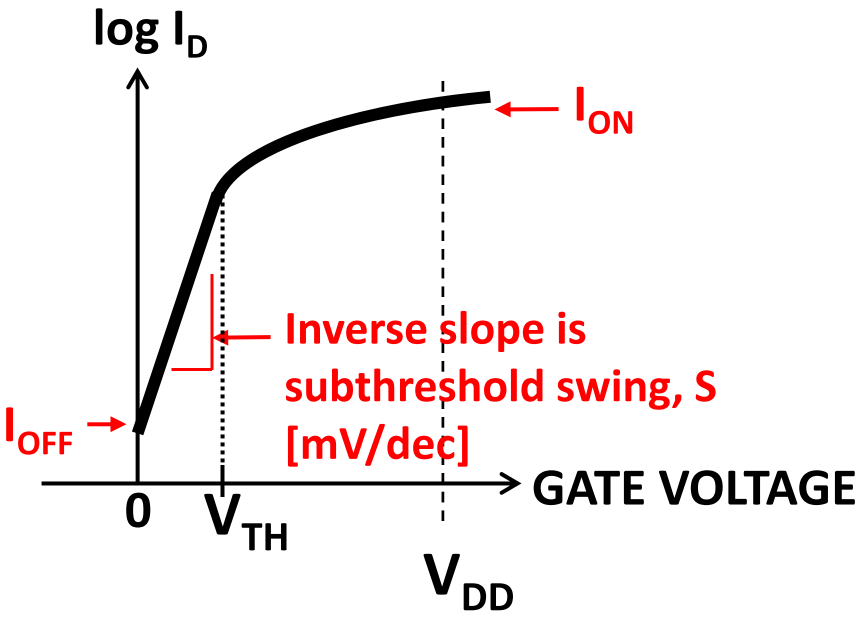
MOSFET Operation: Gate Control

Desired characteristics:
- High ON current
- Low OFF current



- Current between Source and Drain is controlled by the Gate voltage.
- "N-channel" & "P-channel" MOSFETs operate in a complementary manner
  "CMOS" = Complementary MOS





MOSFET in ON State ($V_{GS} > V_{TH}$)

width velocity inversion-layer charge density

$$I_D = W \times v \times Q_{inv}$$

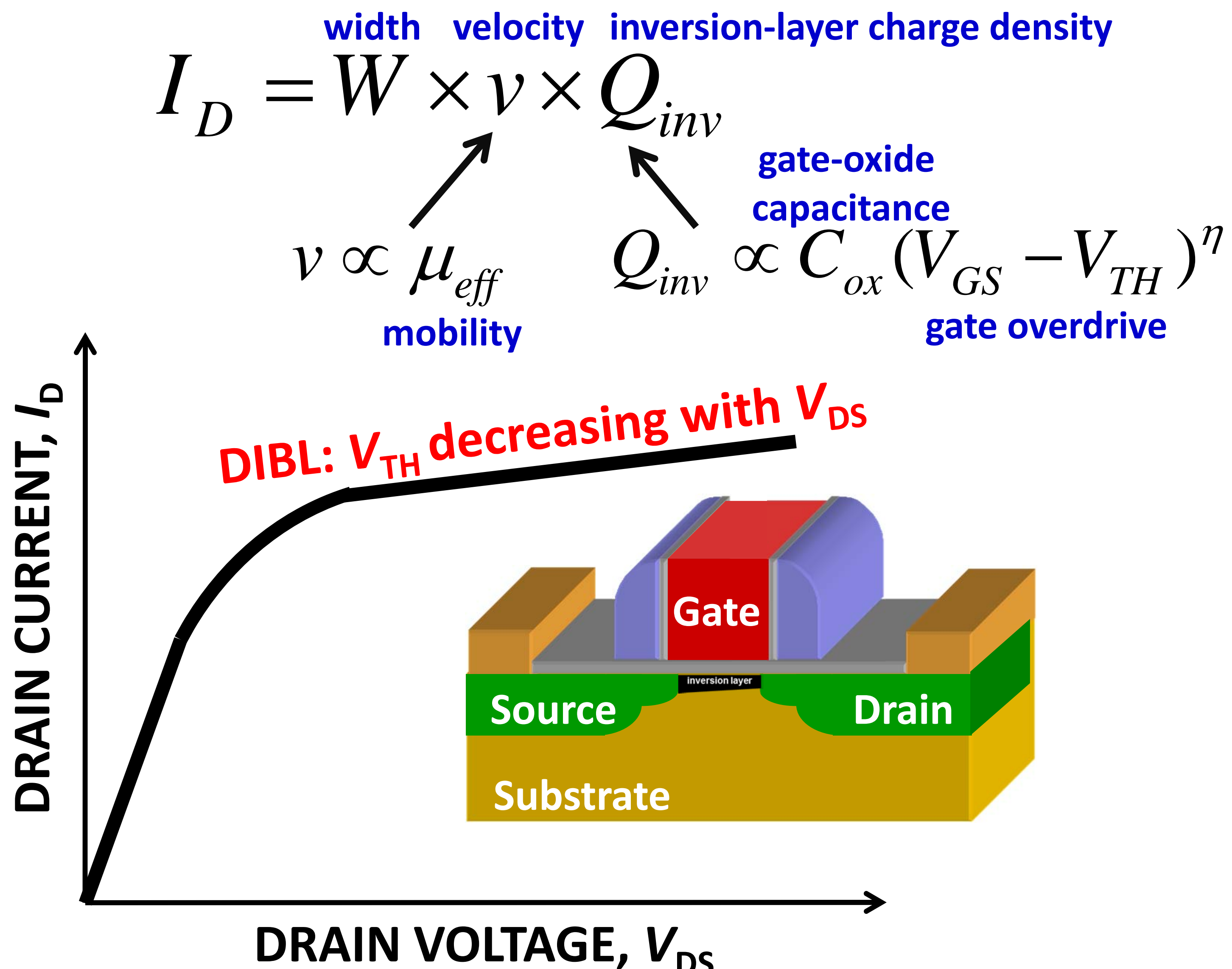
$$v \propto \mu_{eff}$$

mobility

gate-oxide capacitance

$$Q_{inv} \propto C_{ox}(V_{GS} - V_{TH})^{\eta}$$

gate overdrive



CMOS Devices and Circuits

CIRCUIT SYMBOLS

N-channel MOSFET

P-channel MOSFET

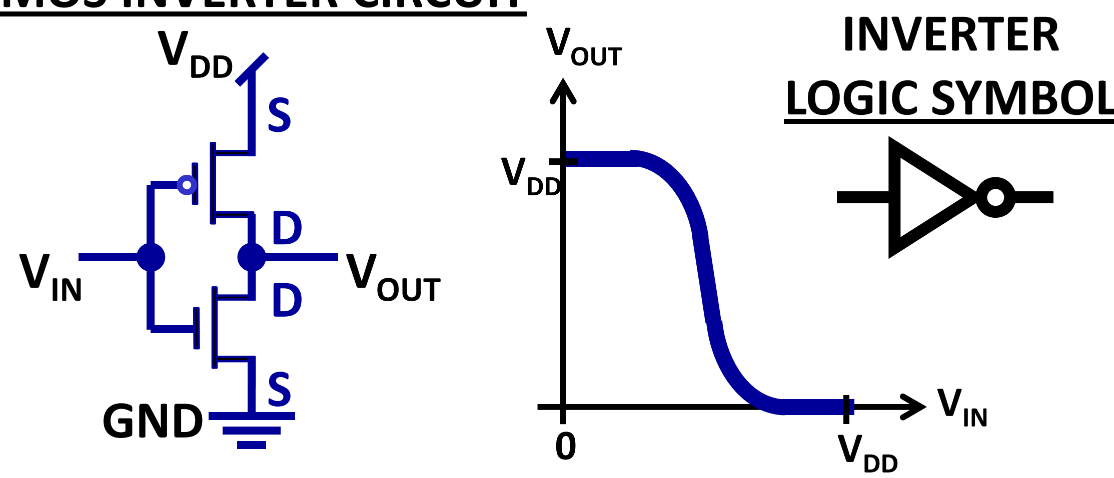
G

S D

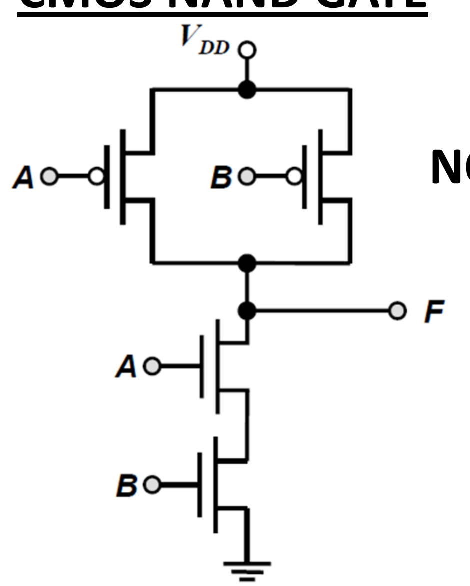
G

S D

CMOS INVERTER CIRCUIT



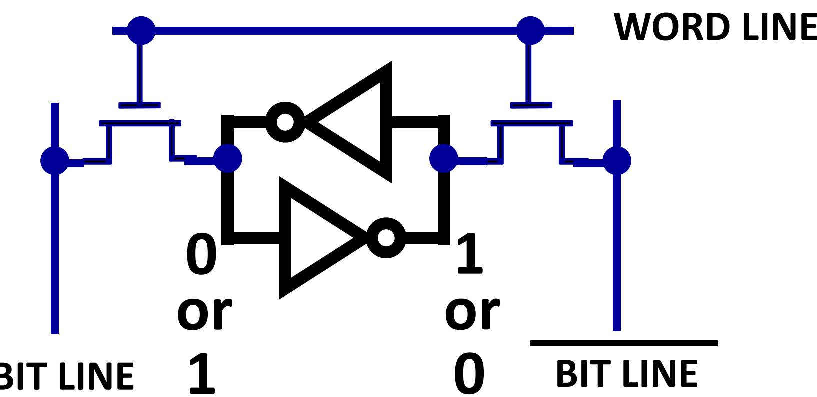
CMOS NAND GATE



NOT AND (NAND) TRUTH TABLE

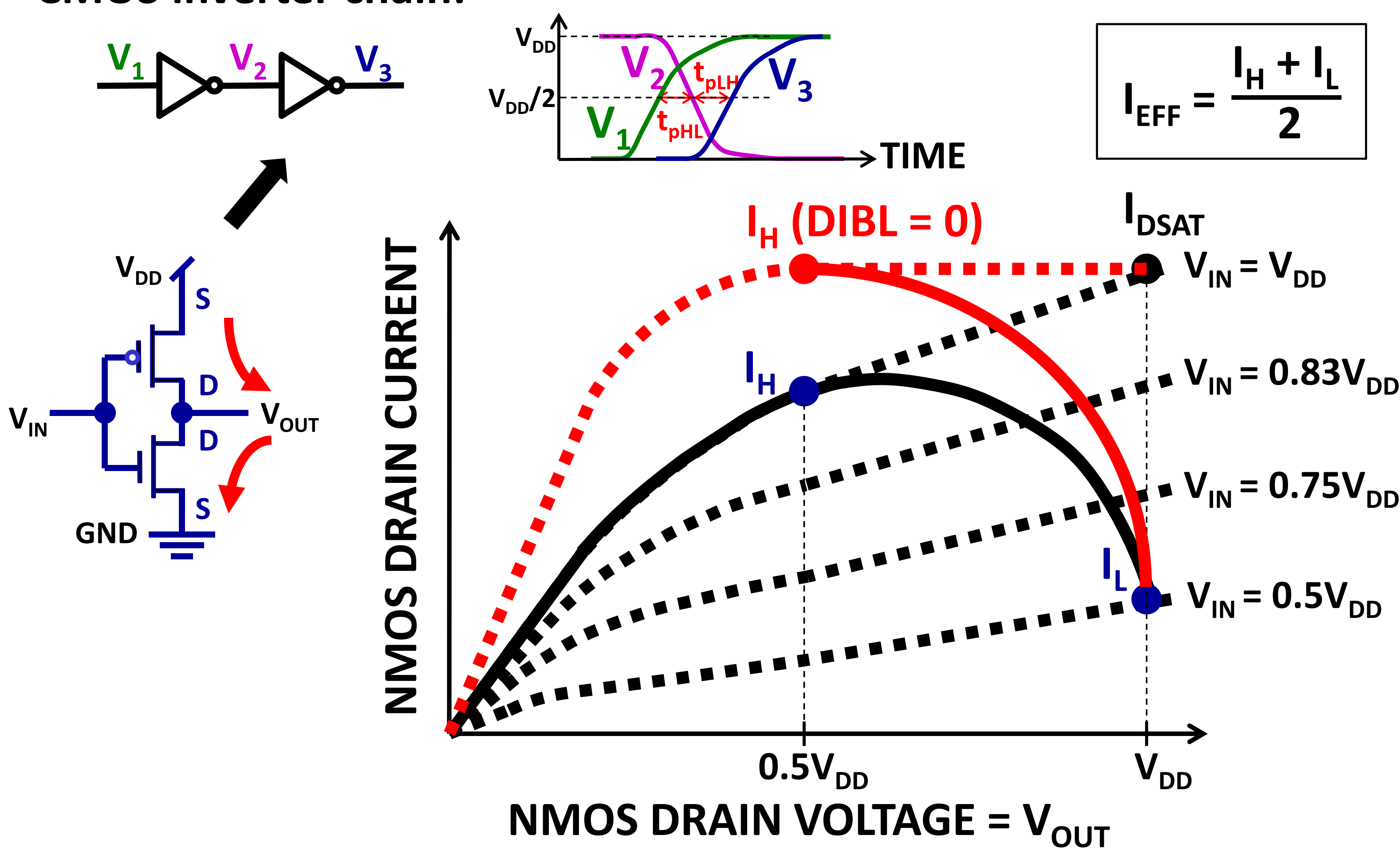
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

STATIC MEMORY (SRAM) CELL



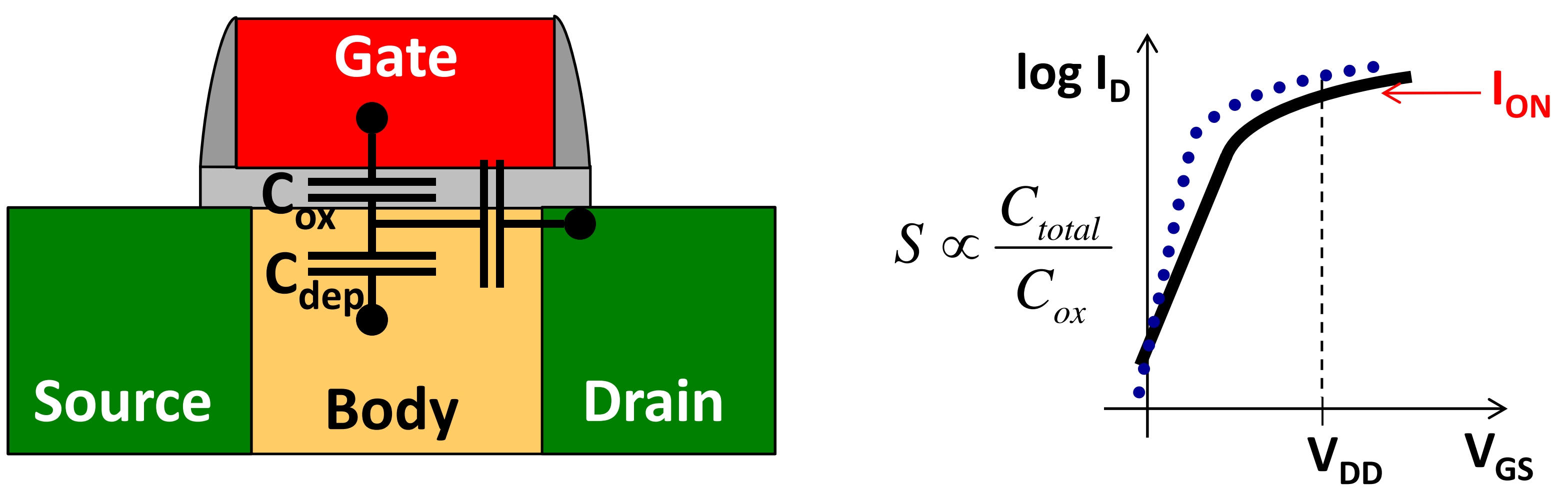
Effective Drive Current (I_{EFF})

CMOS inverter chain:



M. H. Na *et al.*, *IEDM Technical Digest*, pp. 121-124, 2002

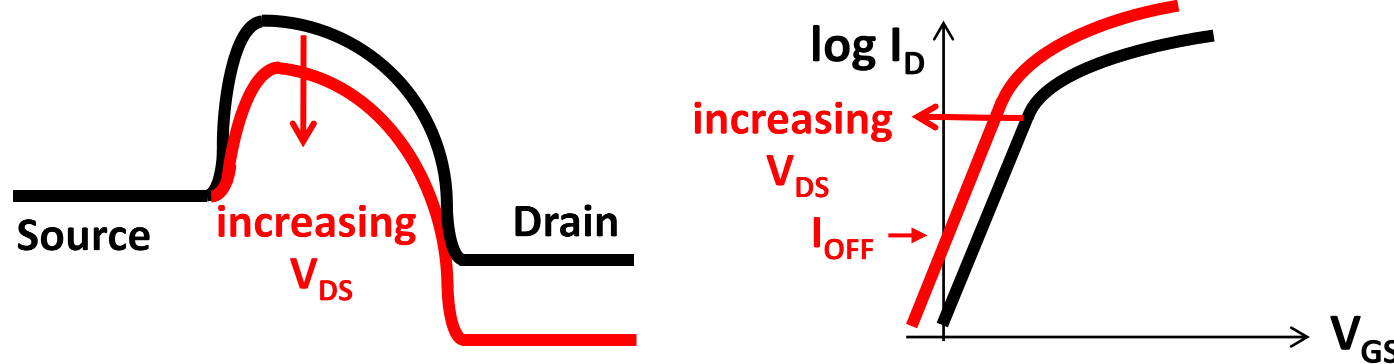
Improving I_{EFF}



- **The greater the capacitive coupling between Gate and channel, the better control the Gate has over the channel potential.**

→higher I_{ON}/I_{OFF} for fixed V_{DD}, or lower V_{DD} to achieve target I_{ON}/I_{OFF}

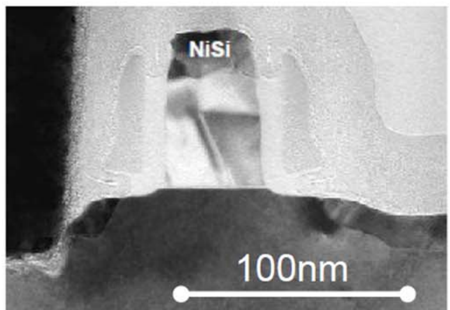
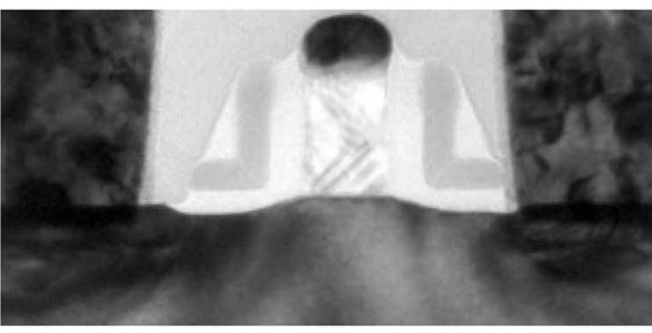
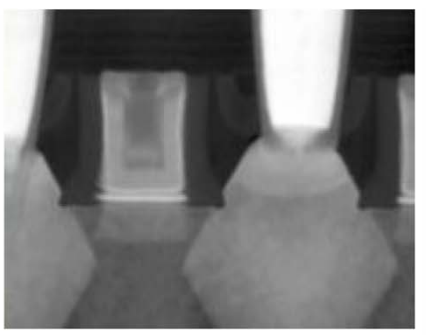
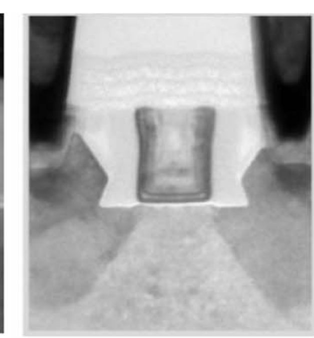
→reduced drain-induced barrier lowering (DIBL):



CMOS Technology Scaling

XTEM images with the same scale

courtesy V. Moroz (Synopsys, Inc.)

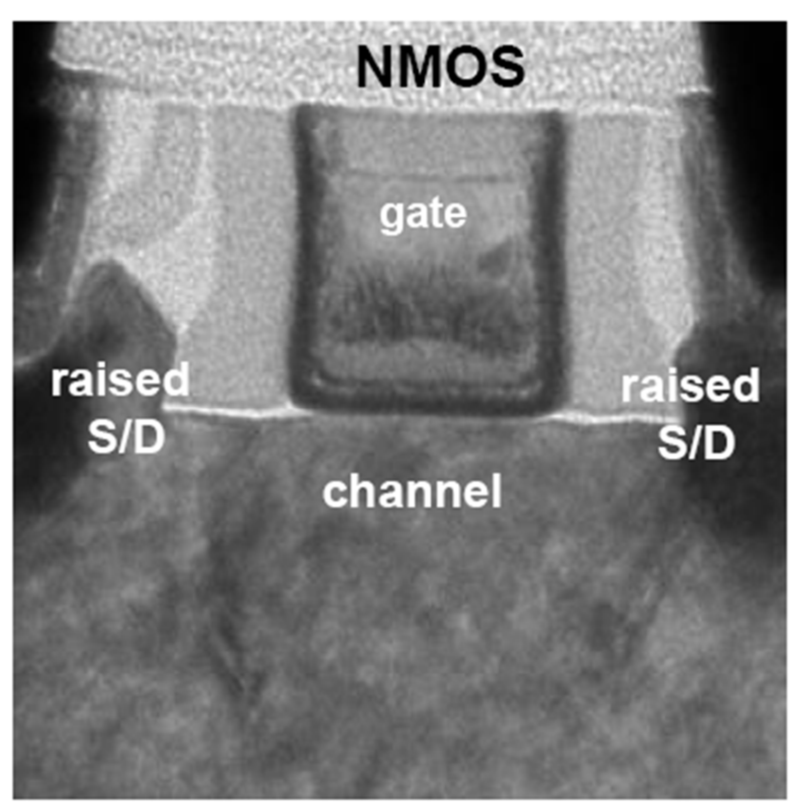
90 nm node	**65 nm node**	**45 nm node**	**32 nm node**
			
T. Ghani *et al*., *IEDM* 2003	(after S. Tyagi *et al*., *IEDM* 2005)	K. Mistry *et al*., *IEDM* 2007	P. Packan *et al*., *IEDM* 2009

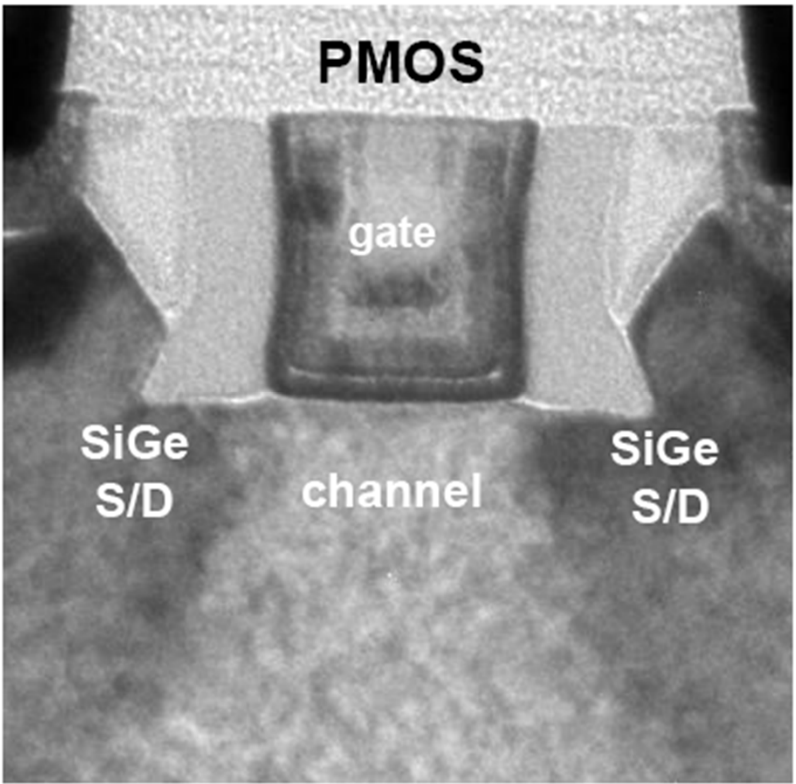
- **Gate length has not scaled proportionately with device pitch (0.7x per generation) in recent generations.**
  - **Transistor performance has been boosted by other means.**

MOSFET Performance Boosters

- **Strained channel regions → $\mu_{eff}\uparrow$**
- **High-k gate dielectric and metal gate electrodes → $C_{ox}\uparrow$**

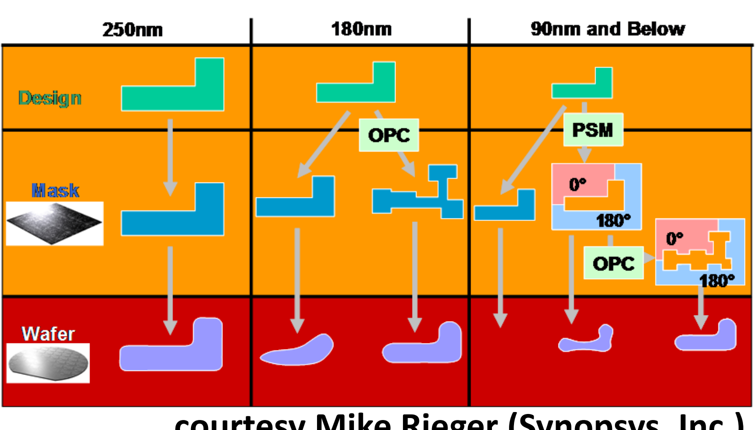
Cross-sectional TEM views of Intel's 32 nm CMOS devices





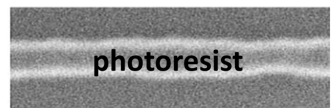
Process-Induced Variations

- **Sub-wavelength lithography:**
  - Resolution enhancement techniques are costly and increase process sensitivity

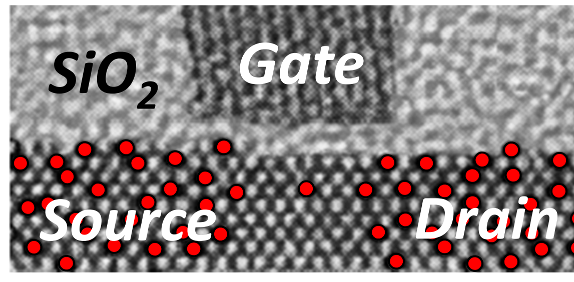


courtesy Mike Rieger (Synopsys, Inc.)

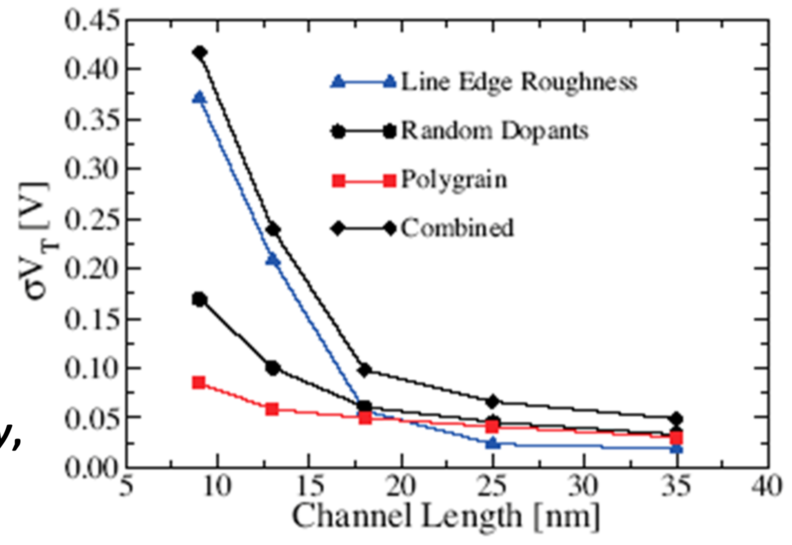
- **Gate line-edge roughness:**



- **Random dopant fluctuations (RDF):**
  - Atomistic effects become significant in nanoscale FETs



A. Brown *et al.*, *IEEE Trans. Nanotechnology*, p. 195, 2002



A. Asenov, *Symp. VLSI Tech. Dig.*, p. 86, 2007

Bulk MOSFET Design Optimization

- To maximize I_{EFF} and minimize V_{TH} variation, heavy doping near the surface of the channel region should be avoided.

→ Use a steep retrograde channel doping profile to suppress I_{OFF}

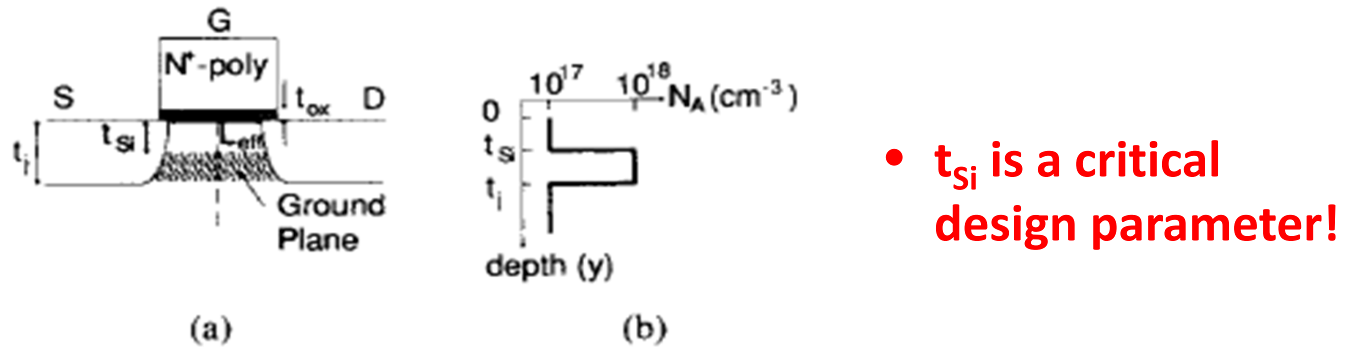
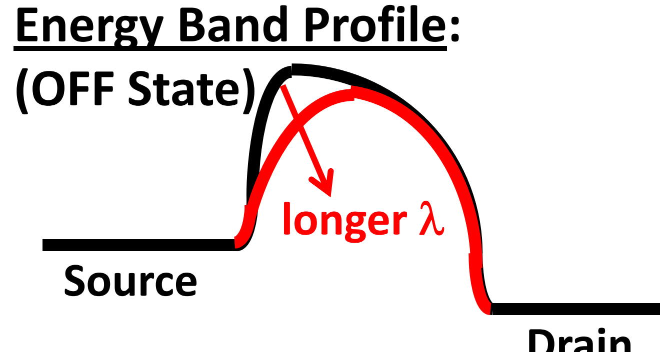


Fig. 6. The Pulse-Shaped Doped structure. (a) Cross-section view of the structure. (b) Vertical doping profile. The example used in Fig. 7 has $L_{eff} = 0.1\ \mu m$, $t_{ox} = 40$ Å, $t_{Si} = 250$ Å, $t_j = 500$ Å, and the doping profile shown in Fig. 6(b).

- t_{Si} is a critical design parameter!

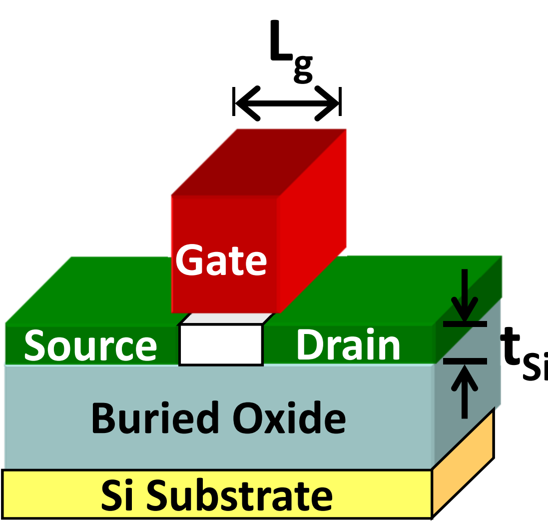
Energy Band Profile:



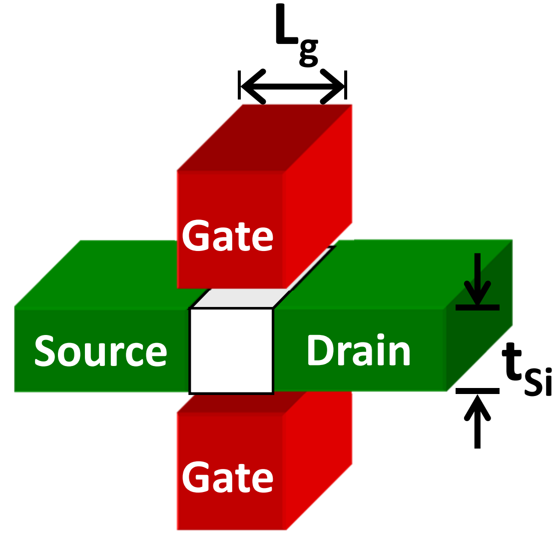
Structure:	Double-Gate FET	Ground-Plane FET
Scale length:	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}} t_{Si} t_{ox}}$	$\lambda = \sqrt{\frac{\varepsilon_{Si}}{2\varepsilon_{ox}} \frac{t_{Si} t_{ox}}{1 + (\varepsilon_{Si} t_{ox} / \varepsilon_{ox} t_{Si})}}$

Thin-Body MOSFETs

Ultra-Thin Body (UTB)



Double-Gate (DG)

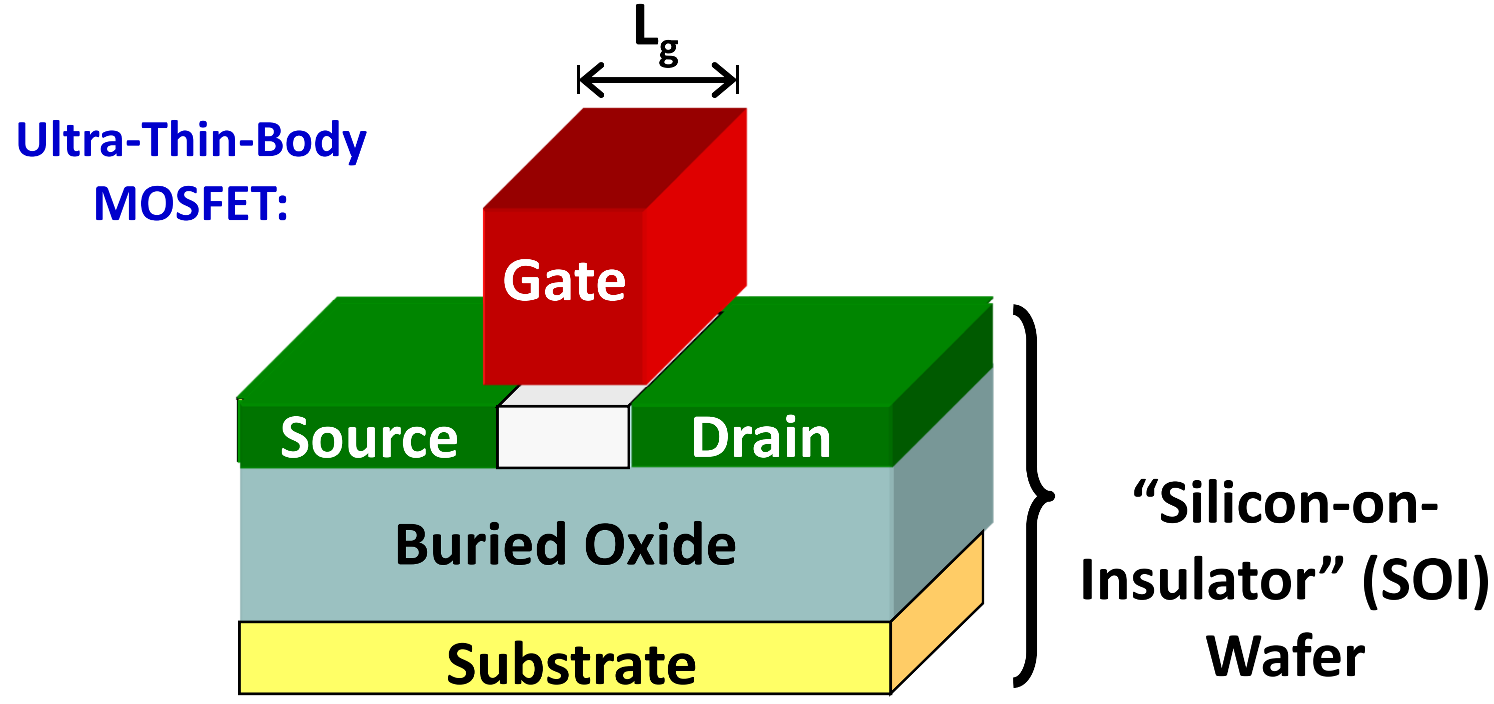


B. Yu *et al.*, *ISDRS* 1997

R.-H. Yan *et al.*, *IEEE TED* 1992

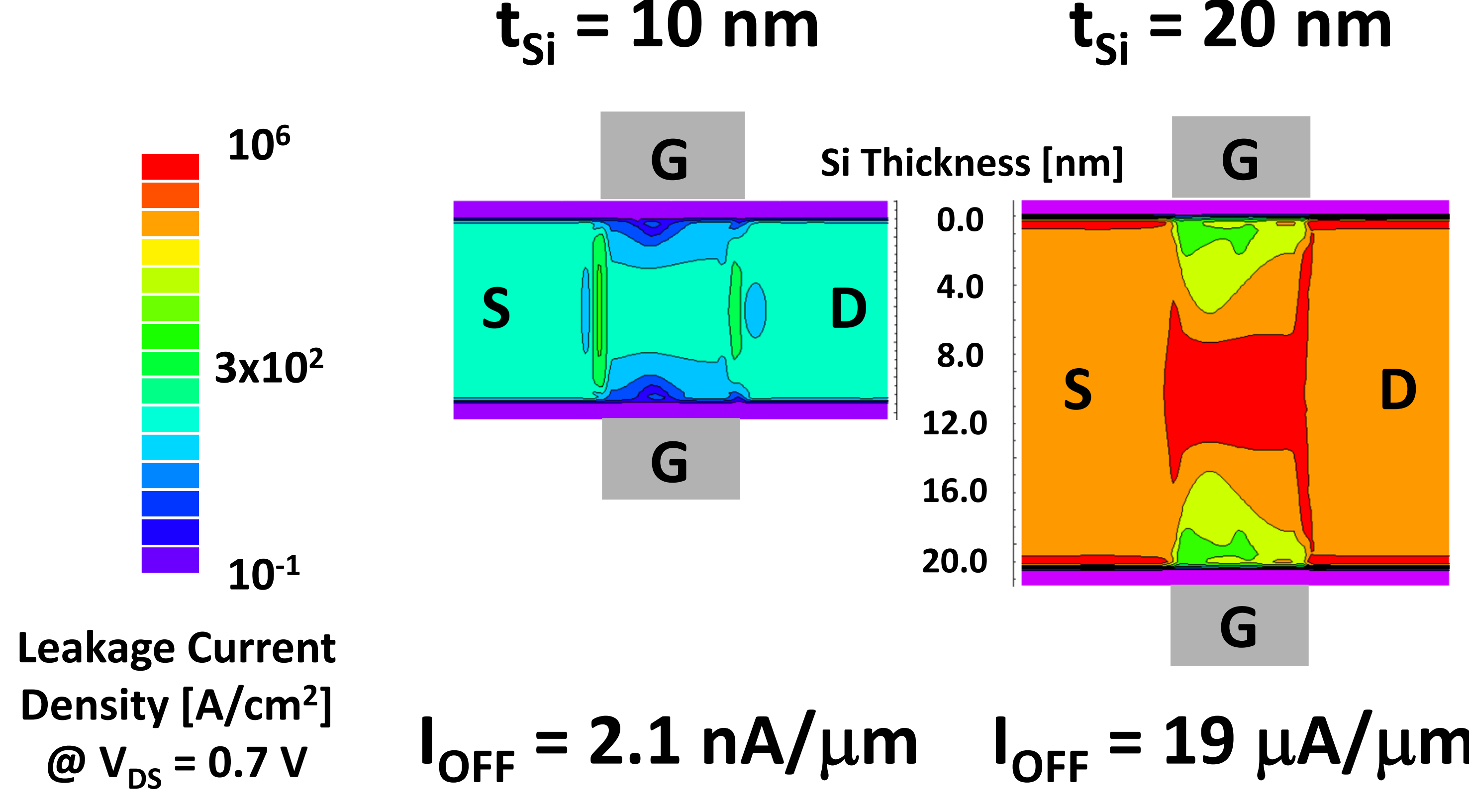
Why Thin-Body Structures?

- Physically limit the depth of the channel region to eliminate sub-surface leakage paths and achieve good electrostatic integrity
- Body doping can be eliminated if t_{Si} is sufficiently thin
  - → higher I_{ON} due to higher carrier mobility
  - → reduced impact of random dopant fluctuations (RDF)



Effect of t_{Si} on OFF-state Leakage

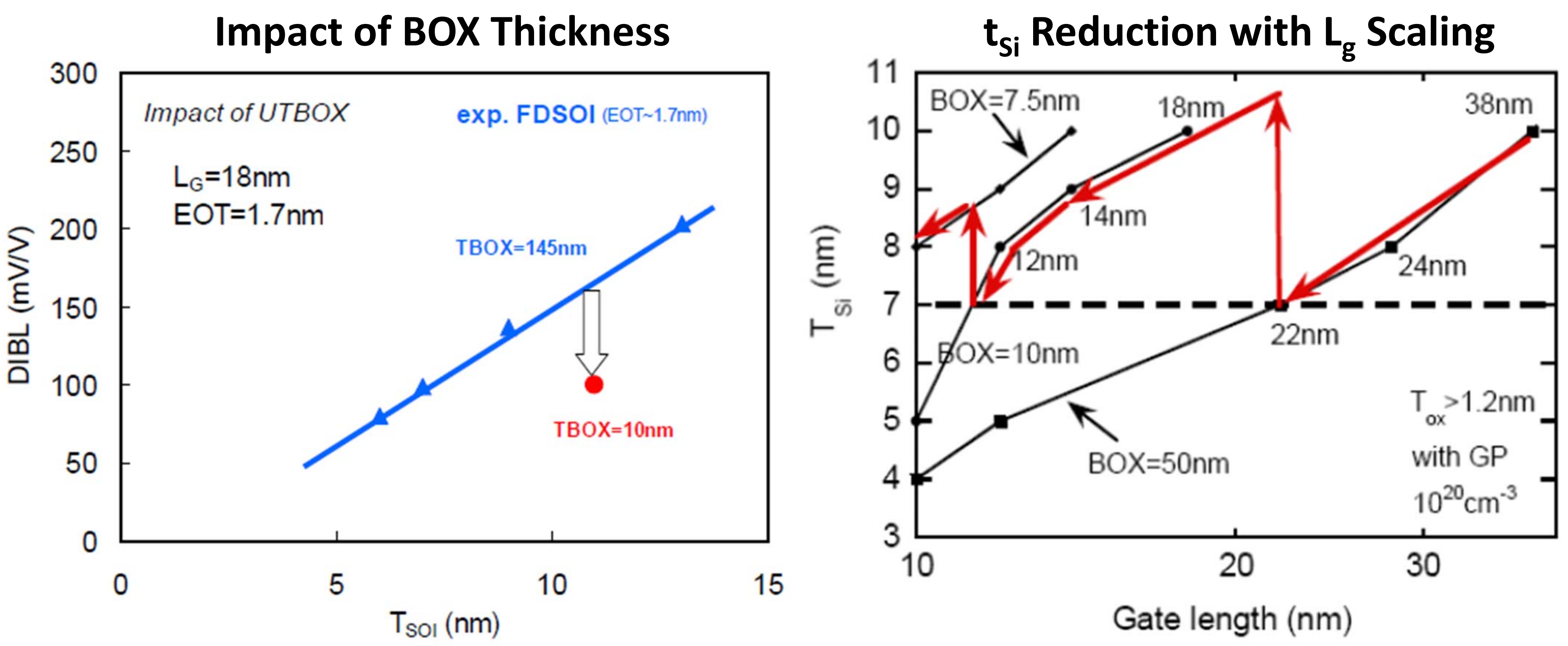
L_g = 25 nm; $t_{ox,eq}$ = 12Å



I_{OFF} = 2.1 nA/μm I_{OFF} = 19 μA/μm

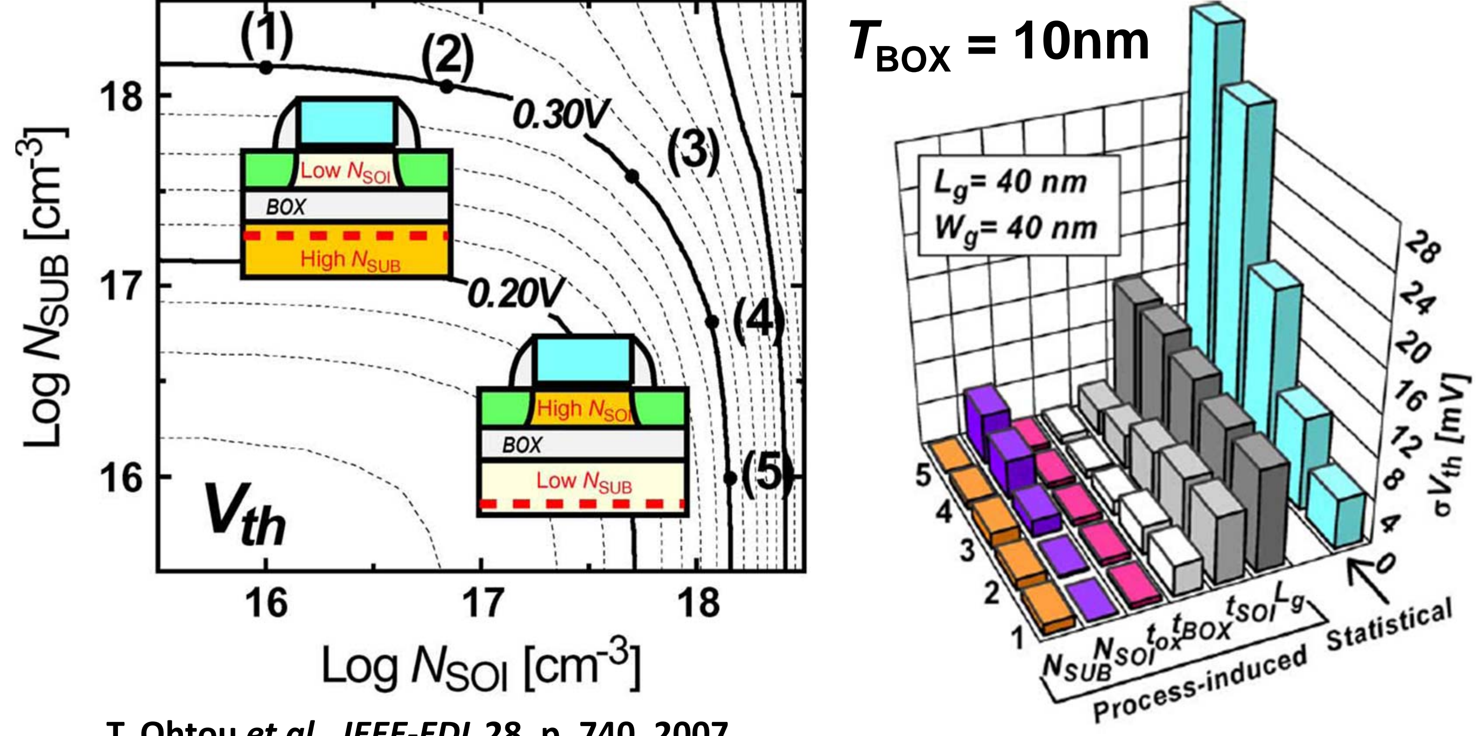
Relaxing the Body Thinness Requirement

- **Thinner buried oxide (BOX) → reduced DIBL**
- **Reverse back biasing → further reduction of SCE**



Threshold Voltage (V_{TH}) Adjustment

- V_{TH} can be adjusted via substrate doping, for reduced σ_{VTH}:

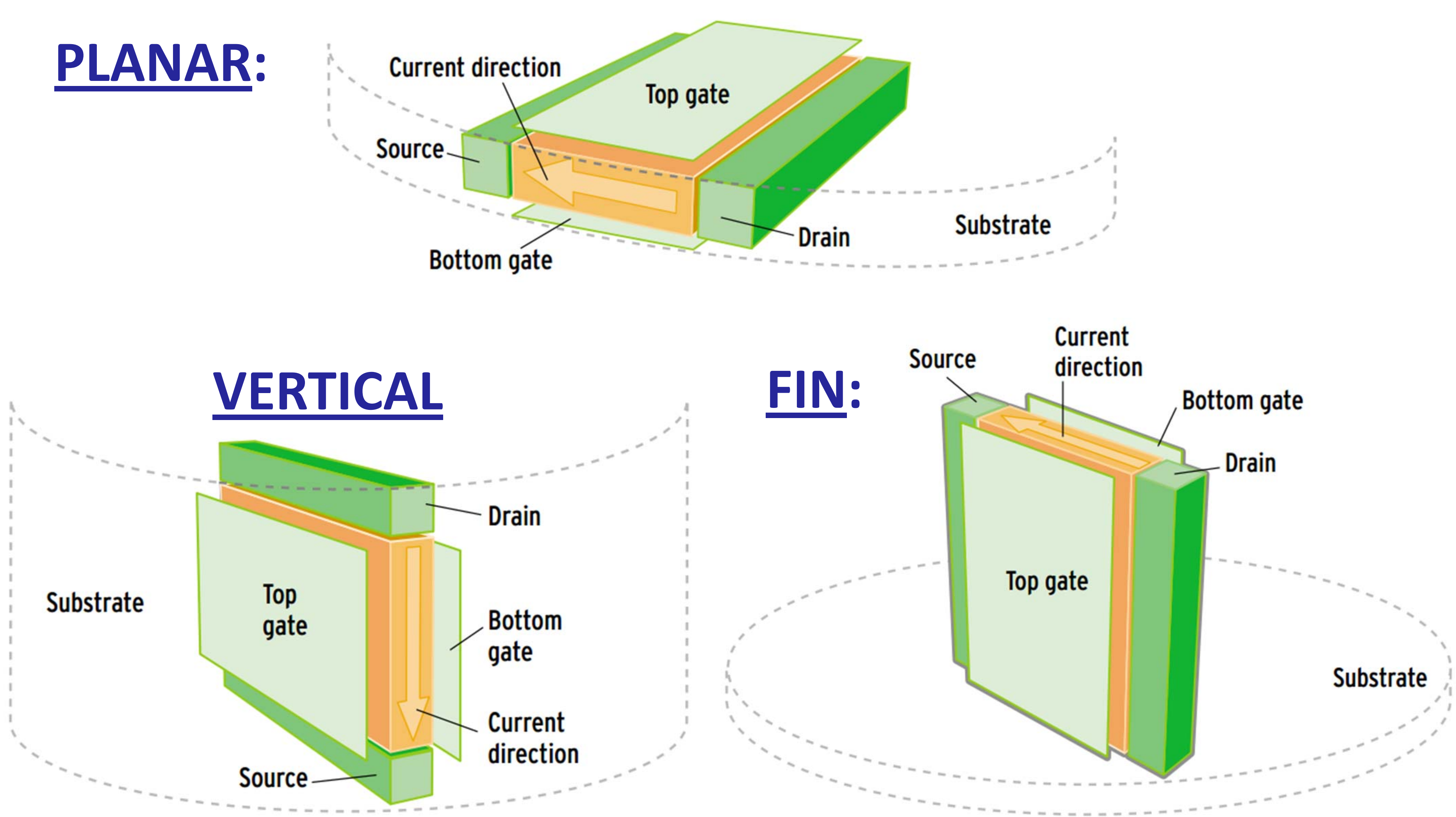


T. Ohtou *et al.*, *IEEE-EDL* 28, p. 740, 2007

- V_{TH} can be dynamically adjusted via back-biasing.
  - Reverse back biasing (to increase V_{TH}) is beneficial for lowering SCE.

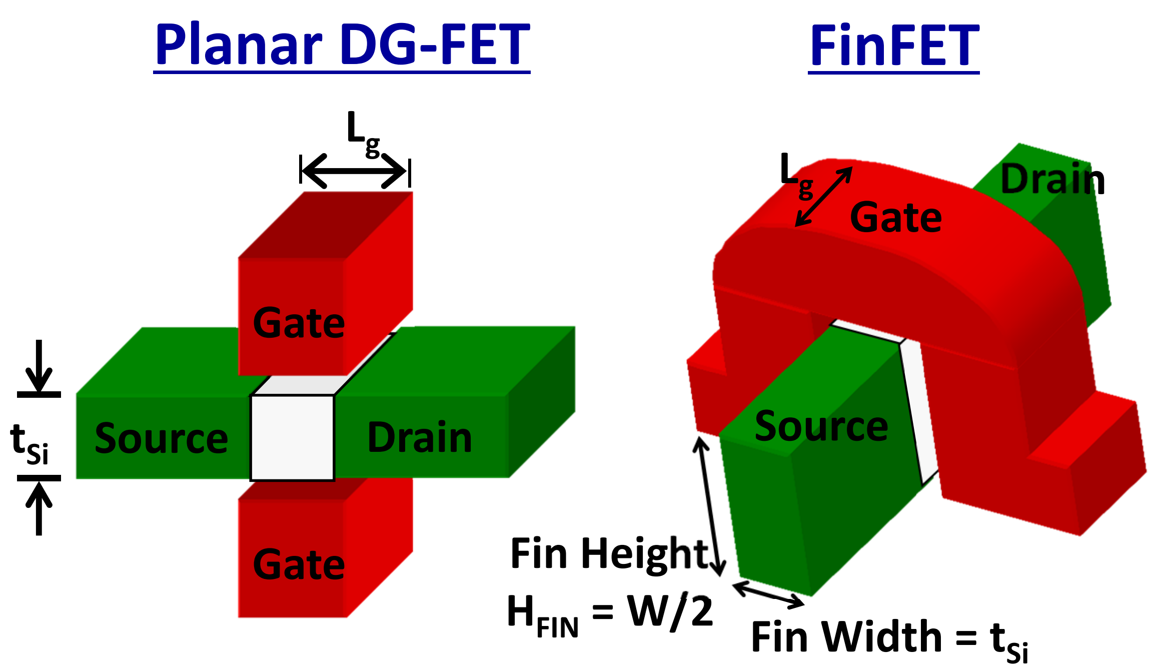
    S. Mukhopadhyay *et al.*, *IEEE-EDL* 27, p. 284, 2006

Double-Gate MOSFET Structures



L. Geppert, *IEEE Spectrum*, October 2002

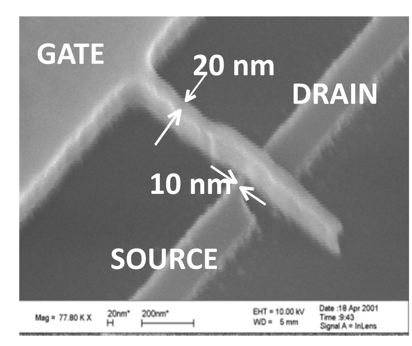
Double-Gate "FinFET"



D. Hisamoto *et al.*, *IEDM Technical Digest*, 1998

N. Lindert *et al.*, *IEEE Electron Device Letters*, p. 487, 2001

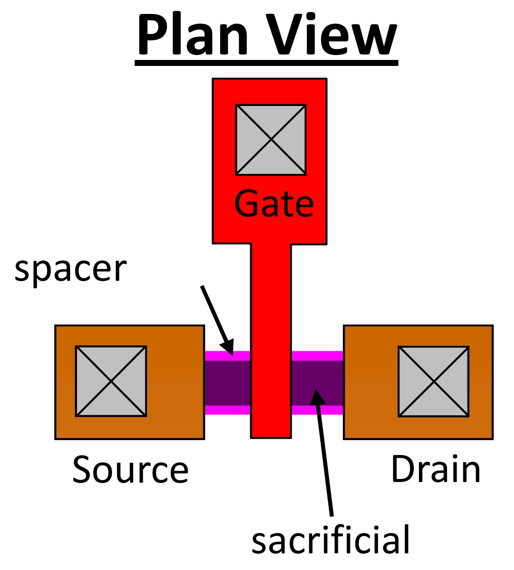
15nm L_g FinFET:



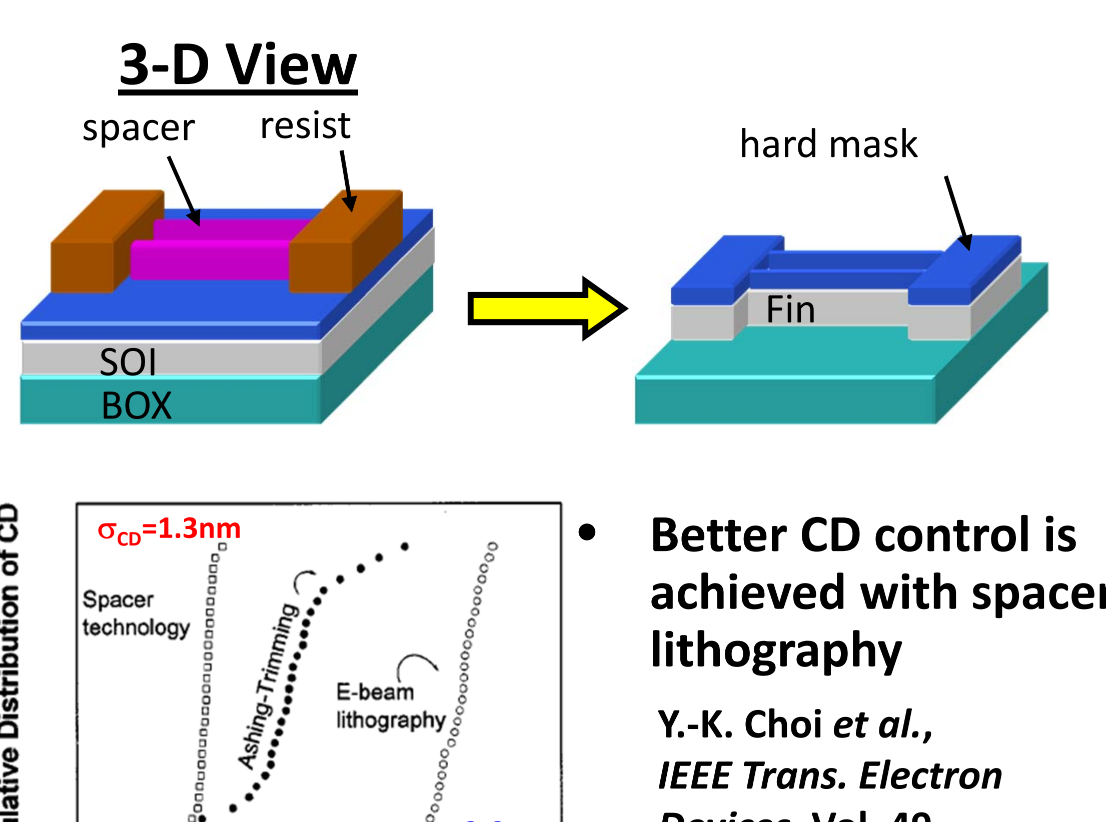
Y.-K. Choi *et al.*, *IEDM Technical Digest*, 2001

Fin Patterning by Spacer Lithography

- **Use spacers to define fins, and photoresist to define source/drain contact pad regions:**



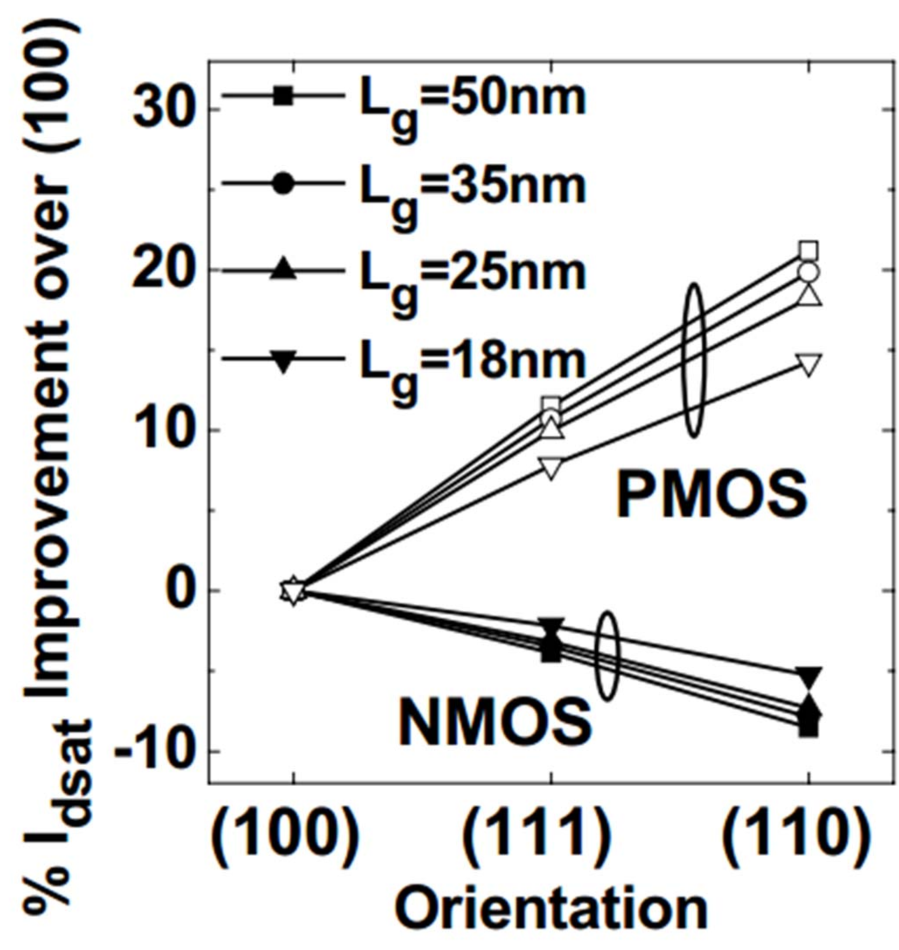
- **Note that gate line-edge roughness is not an issue for FinFETs**



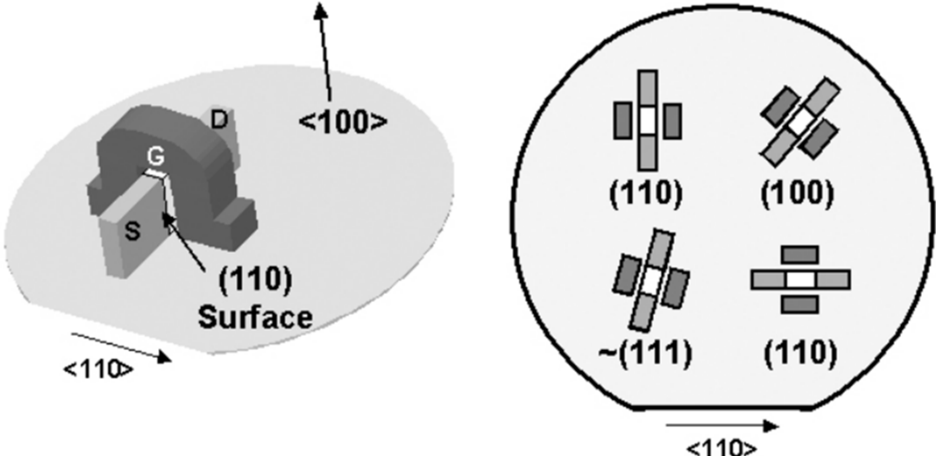
- **Better CD control is achieved with spacer lithography**

Y.-K. Choi *et al.*, *IEEE Trans. Electron Devices*, Vol. 49, pp. 436-441, 2002

Impact of Fin Layout Orientation



(Series resistance is more significant at shorter L_g.)

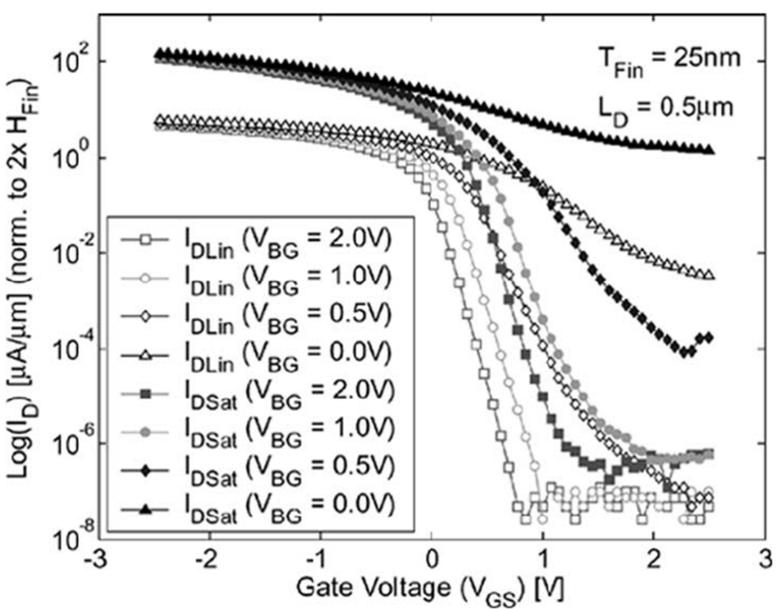


- If the fin is oriented || or ⊥ to the wafer flat, the channel surfaces lie along (110) planes.
  - Lower electron mobility
  - Higher hole mobility
- If the fin is oriented 45° to the wafer flat, the channel surfaces lie along (100) planes.

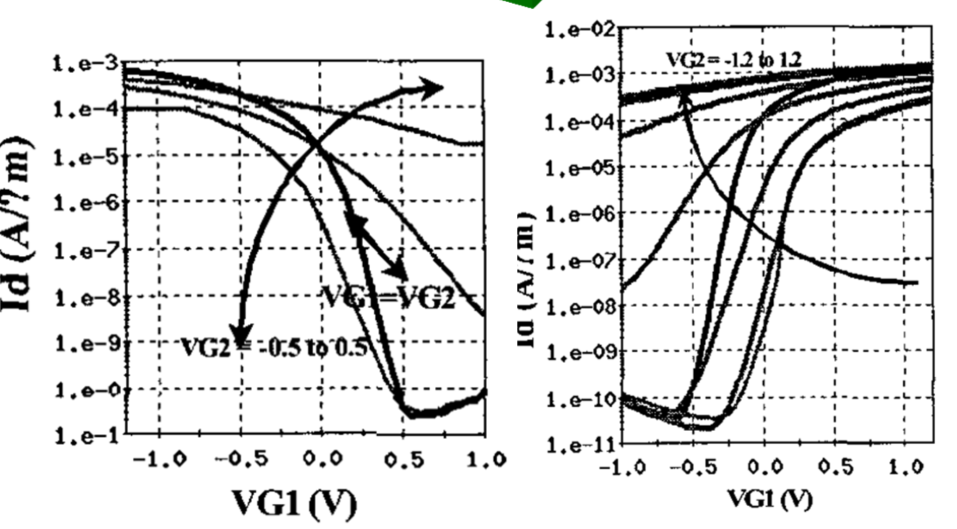
Independent Gate Operation

- **The gate electrodes of a double-gate FET can be isolated by a masked etch, to allow for separate biasing.**
  - **One gate is used for switching.**
  - **The other gate is used for V_{TH} control.**

Drain
Gate1
Gate2
Source
Back-Gated FET



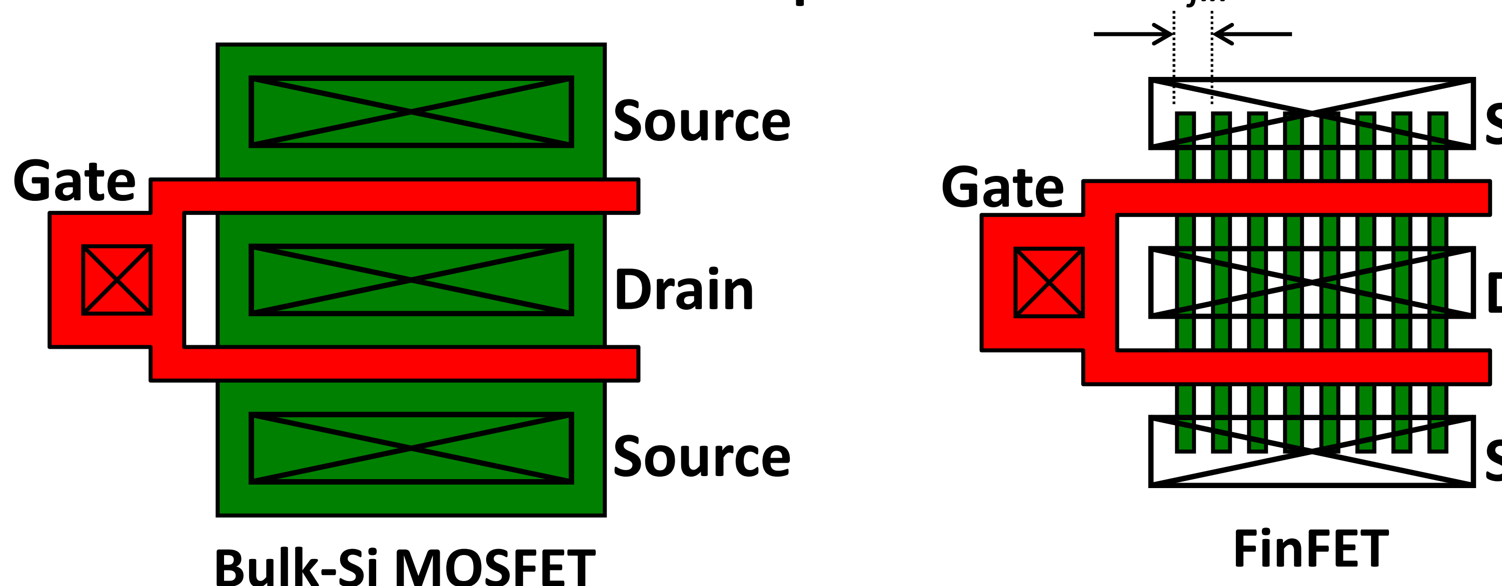
D. M. Fried *et al*. (Cornell U.), *IEEE Electron Device Letters,* Vol. 25, *pp.* 199-201, 2004



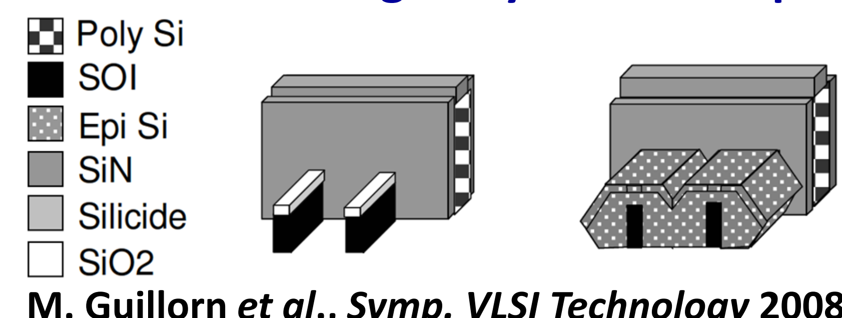
L. Mathew *et al.* (Freescale Semiconductor), *2004 IEEE International SOI Conference*

FinFET Layout

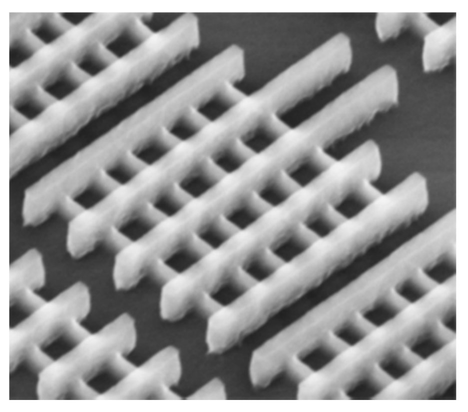
- **Layout is similar to that of conventional MOSFET, except that the channel width is quantized:**



The S/D fins can be merged by selective epitaxy:



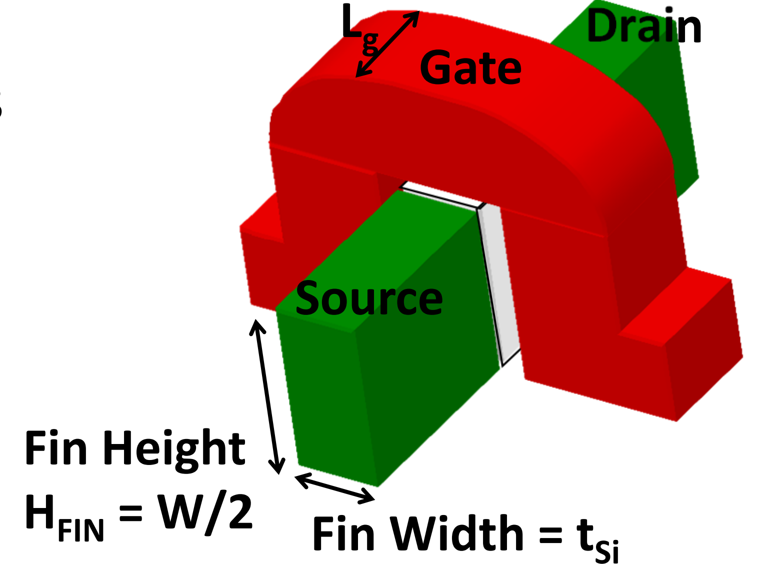
M. Guillorn *et al.*, *Symp. VLSI Technology* 2008

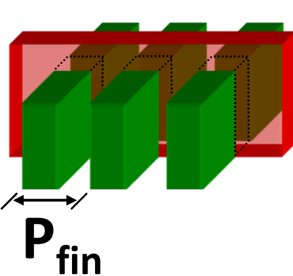


Intel Corp.

FinFET Design Trade-Offs

- **Fin Width**
  - Determines short-channel effects
- **Fin Height**
  - Limited by etch technology
  - Tradeoff: layout efficiency *vs.* design flexibility
- **Fin Pitch**
  - Limited by lithographic capability
  - Constrains source/drain implant tilt angle
  - Tradeoff: performance *vs.* layout efficiency

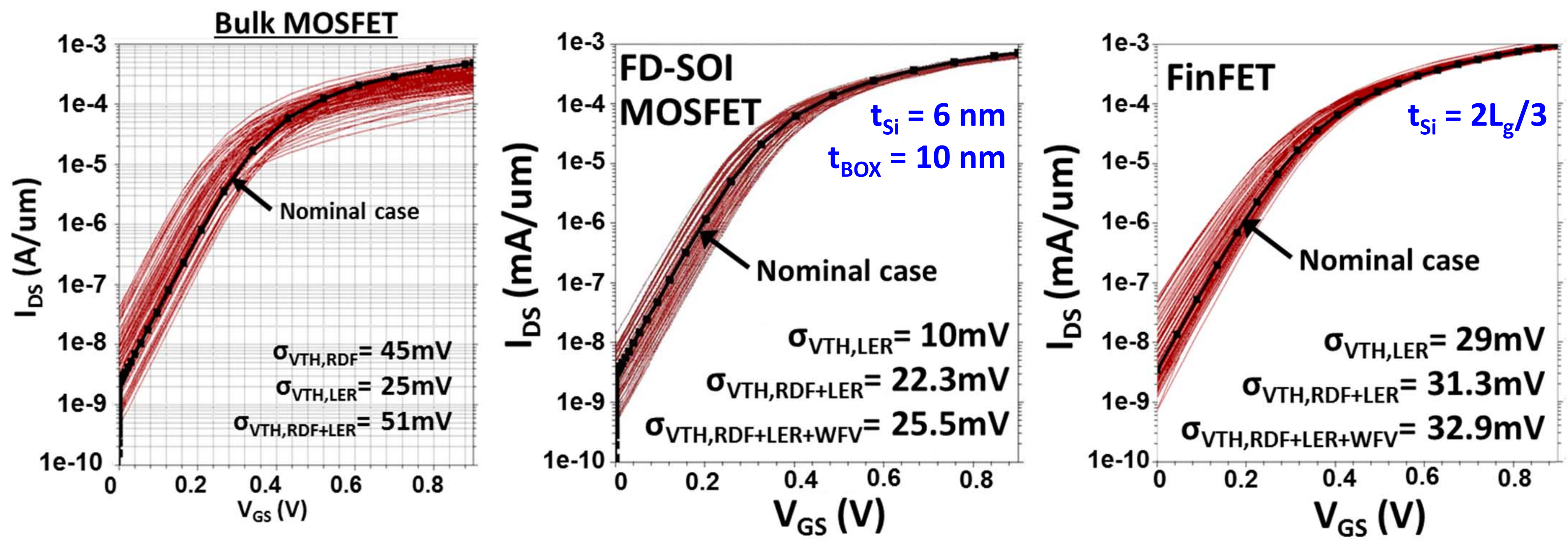




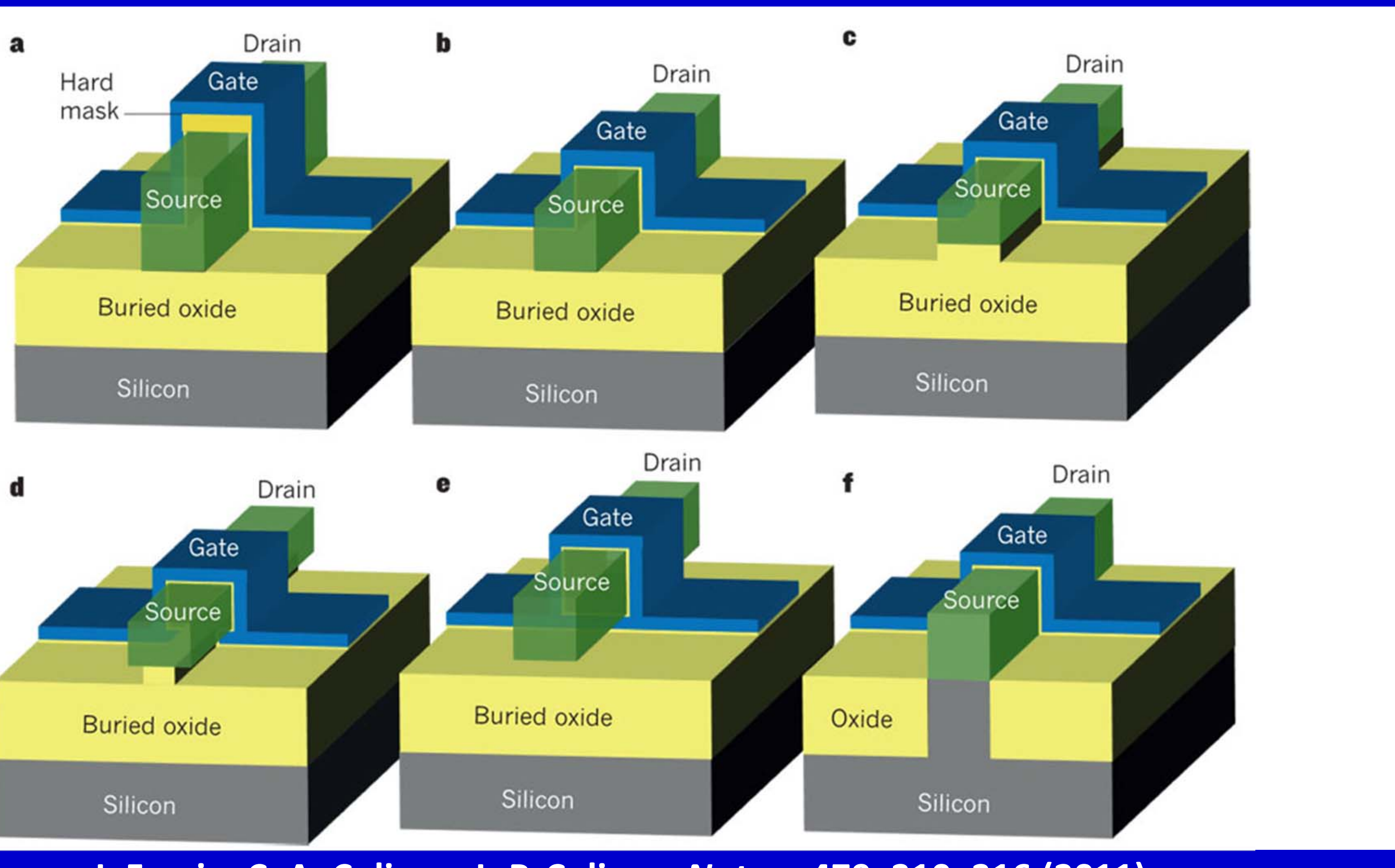
Parasitic gate resistance and capacitance depend on P_{fin}

Impact of Random Variations @ 25 nm L_g

- RDF-induced variations were simulated using KMC model
- Gate-LER-induced variations were simulated by sampling profiles from an SEM image of a photoresist line
- Φ_M variations were estimated based on Dadgour *et al.*, *2008 IEDM*

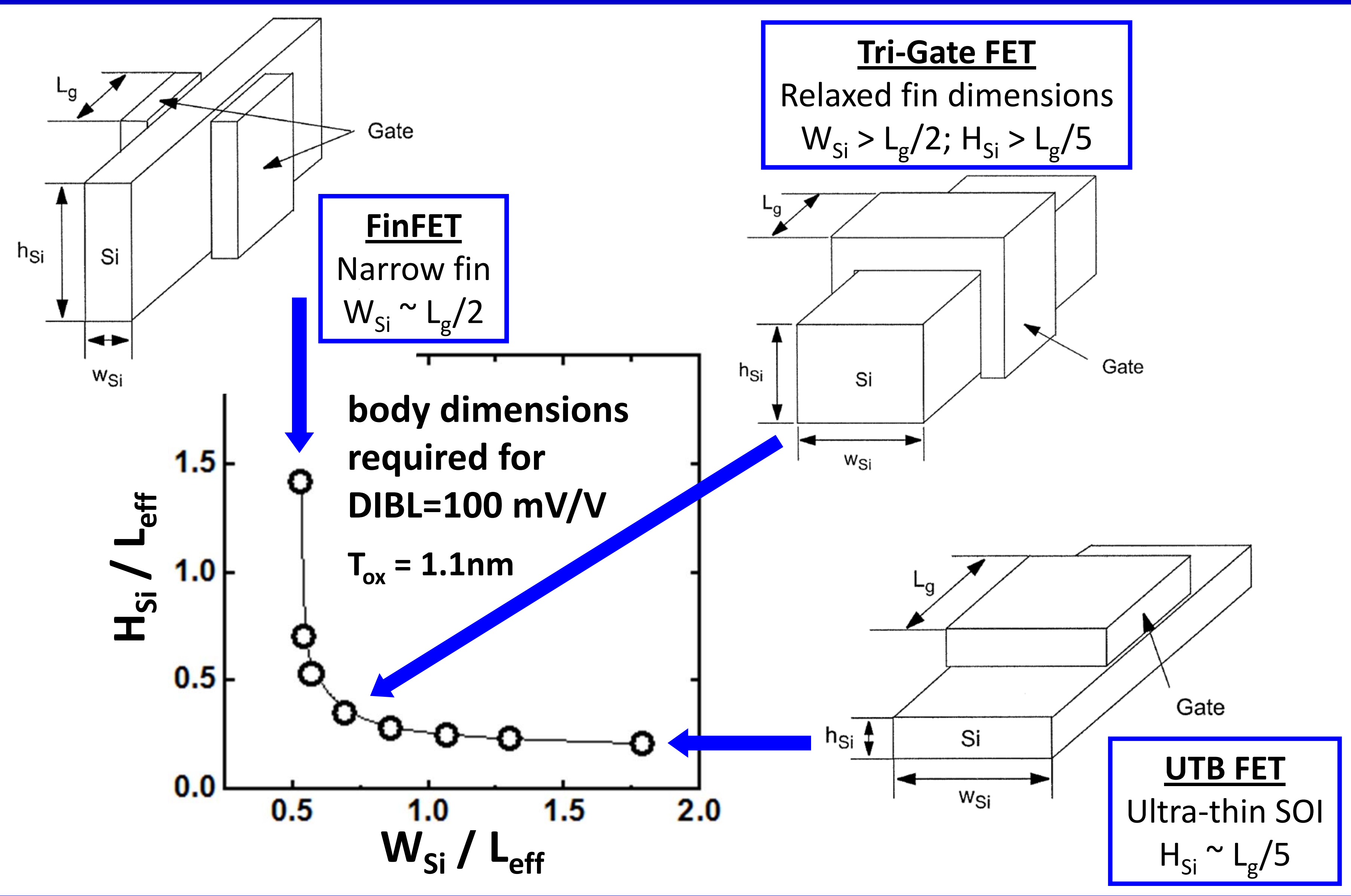


Multi-gate MOSFETs



I. Ferain, C. A. Colinge, J.-P. Colinge, *Nature* 479, 310–316 (2011)

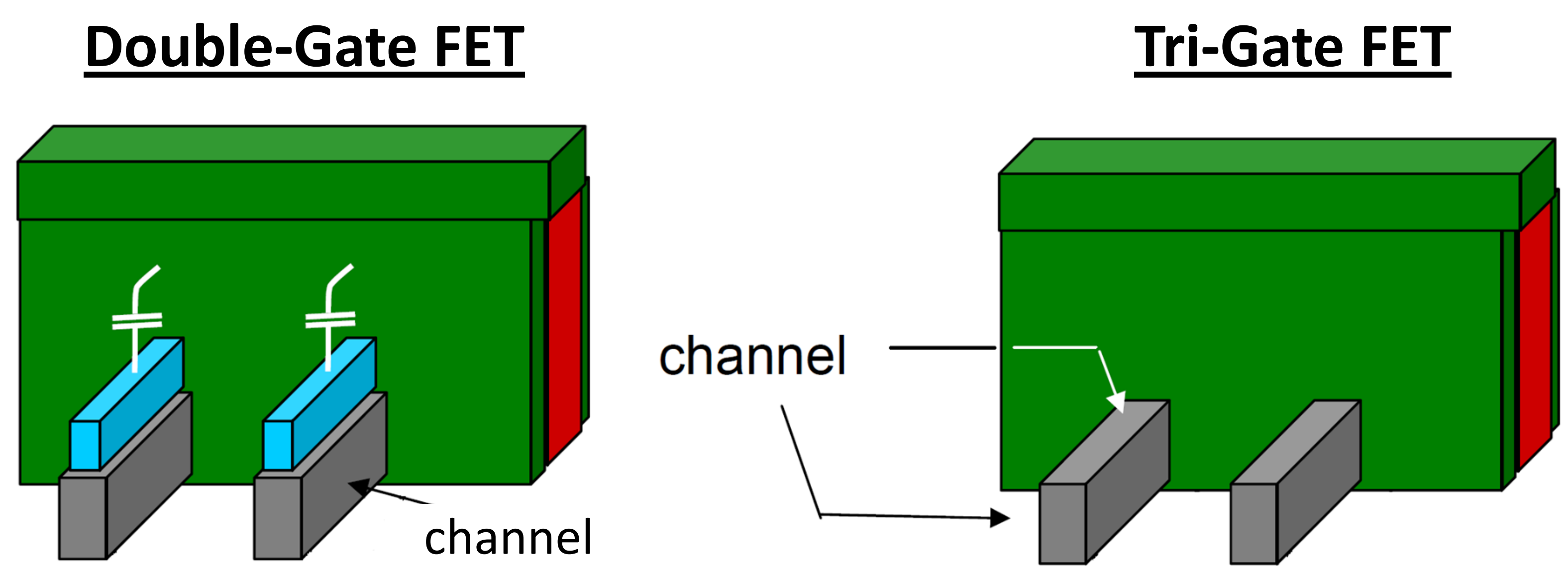
SOI Multi-Gate MOSFET Designs



after Yang and Fossum, *IEEE Trans. Electron Devices*, Vol. 52, pp. 1159-1164, 2005

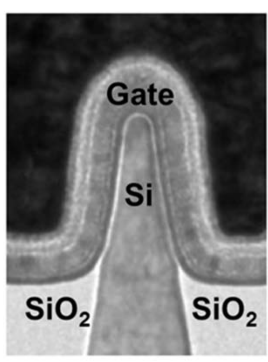
Double-Gate *vs.* Tri-Gate FET

- The Double-Gate FET does not require a highly selective gate etch, due to the protective dielectric hard mask.
- Additional gate fringing capacitance is less of an issue for the Tri-Gate FET, since the top fin surface contributes to current conduction in the ON state.



22nm Tri-Gate FETs

- L_g = 30-34 nm; W_{fin} = 8 nm; H_{fin} = 34 nm
- High-k/metal gate stack, EOT = 0.9 nm
- Channel strain techniques



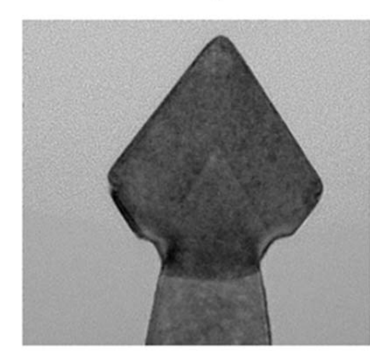
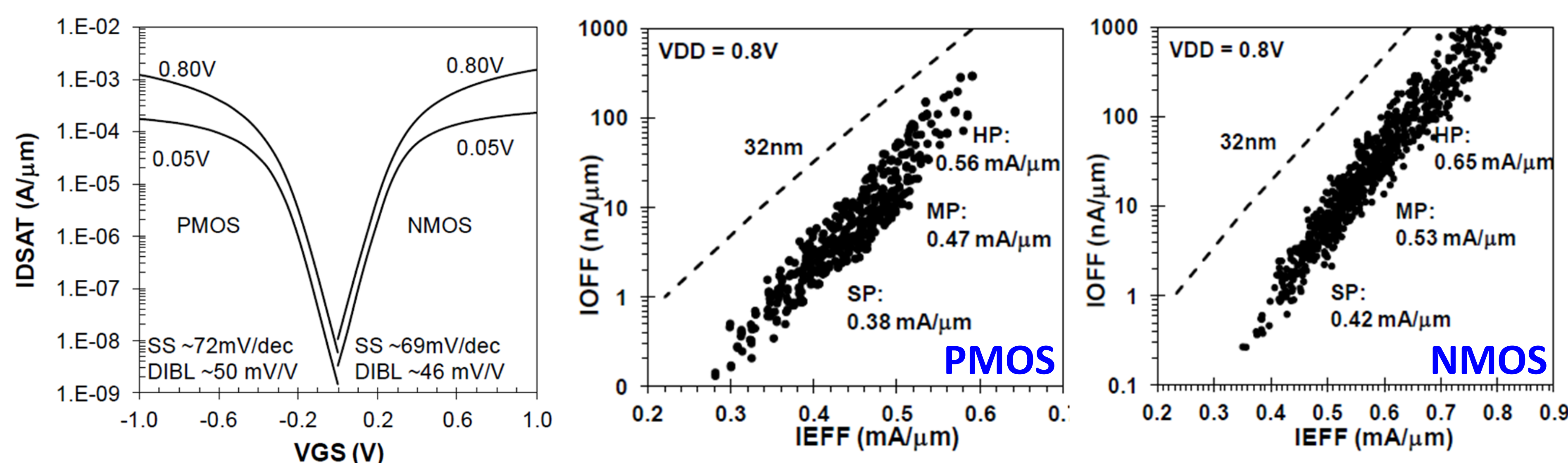


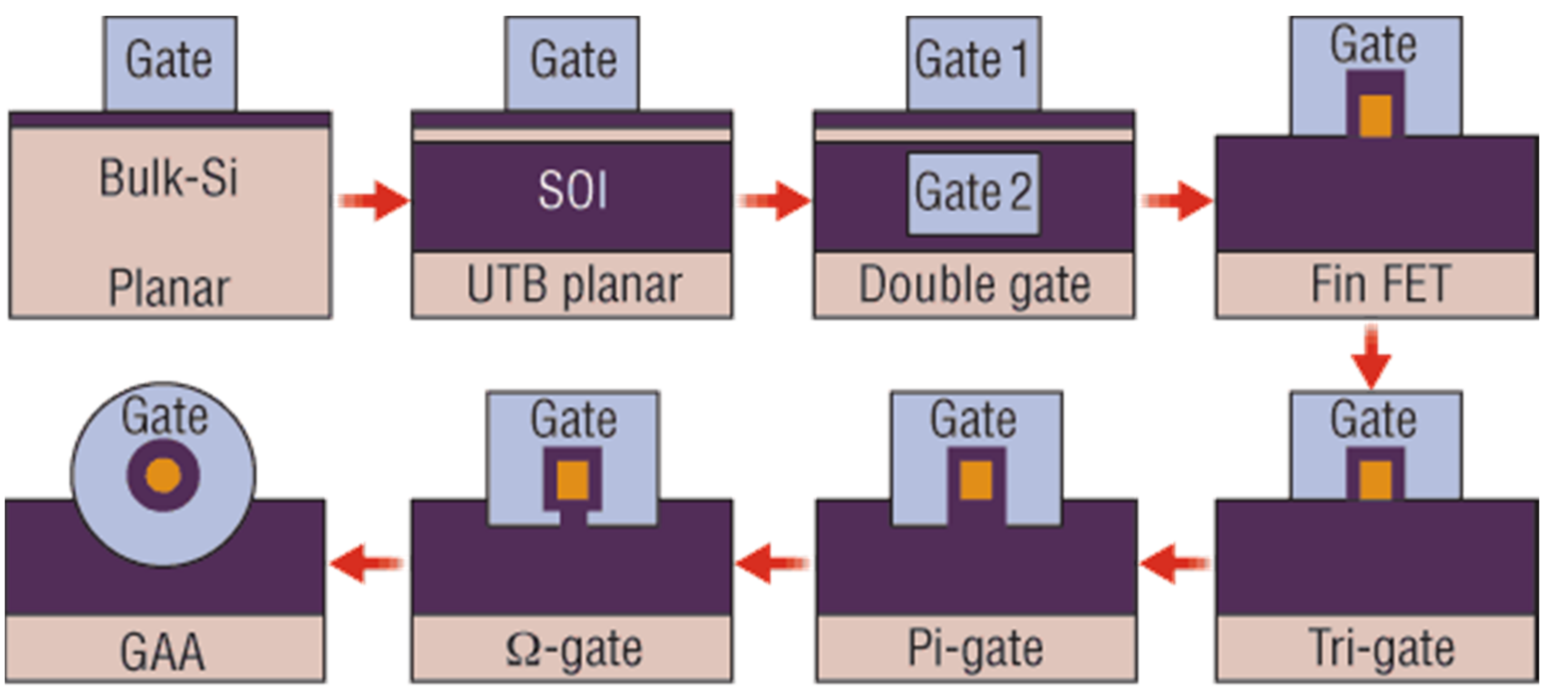
Fig.2 TEMs of the PMOS channel under the gate (left) and in the S/D region (right) showing the SiGe epitaxy in the S/D region.

Transfer Characteristics



SOI MOSFET Evolution

- **The gate-all-around (GAA) structure provides for the greatest capacitive coupling between the gate and the channel.**



http://www.electroiq.com/content/eiq-2/en/articles/sst/print/volume-51/issue-5/features/nanotechnology/fully-gate-all-around-silicon-nanowire-cmos-devices.html

Summary

- **Power density and variability now limit conventional bulk MOSFET scaling.**
- **Multi-gate MOSFET structures can achieve superior electrostatic integrity than the conventional planar bulk MOSFET structure and hence offer a pathway to lower V_{DD}, reduce V_{TH} variability, and extend transistor scaling.**