Design Rules for NMOS

- Design Rules
- Stick Diagrams
- Layout Diagram
- Examples

Design Rules: Introduction

- Design rules are a set of geometrical specifications that dictate the design of the layout
- **Layout is top view of a chip.**
- Design process are aided by stick diagram and layout
- Stick diagram gives the placement of different components and their connection details
- But the dimensions of devices are not mentioned
- Circuit design with all dimensions is Layout

Design Rules: Introduction

- Fabrication process needs different masks, these masks are prepared from layout
- Layout is an Interface between circuit designer and fabrication engineer
- Layout is made using a set of design rules.
- Design rules allow translation of circuit (usually in stick diagram or symbolic form) into actual geometry in silicon wafer
- These rules usually specify the minimum allowable line widths for physical objects on-chip
- Example: metal, polysilicon, interconnects, diffusion areas, minimum feature dimensions, and minimum allowable separations between two such features.

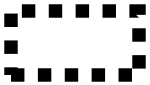
NEED FOR DESIGN RULES

- Better area efficiency
- Better yield
- Better reliability
- Increase the probability of fabricating a successful product on Si wafer

If design rules are not followed:

- Functional or non-functional circuit.
- Design consuming larger Si area.
- The device can fail during or after simulation.

Colour Codes :

Layer	Color	Representation
N+ Active	Green	
P+ Active	Yellow/Brown	
PolySi	Red	
Metal 1	Blue	
Metal 2	Magenta	
Contact	Black	X
Buried contact	Brown	X
Via	Black	X
Implant	Dotted yellow	
N-Well	Dotted Green/Black	

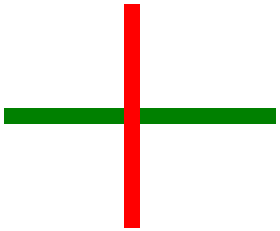
Stick Diagrams :

- A stick diagram is a symbolic representation of a layout.
- In stick diagram, each conductive layer is represented by a line of distinct color.
- Width of line is not important, as stick diagrams just give only wiring and routing information.
- Does show all components/vias, relative placement.
- Does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries.

Stick Diagrams: Basic Rules

- Poly crosses diffusion forms transistor
- Red (poly) over Green(Active), gives a FET.

L:W



nFET/
nMOS

- Aspect Ratio

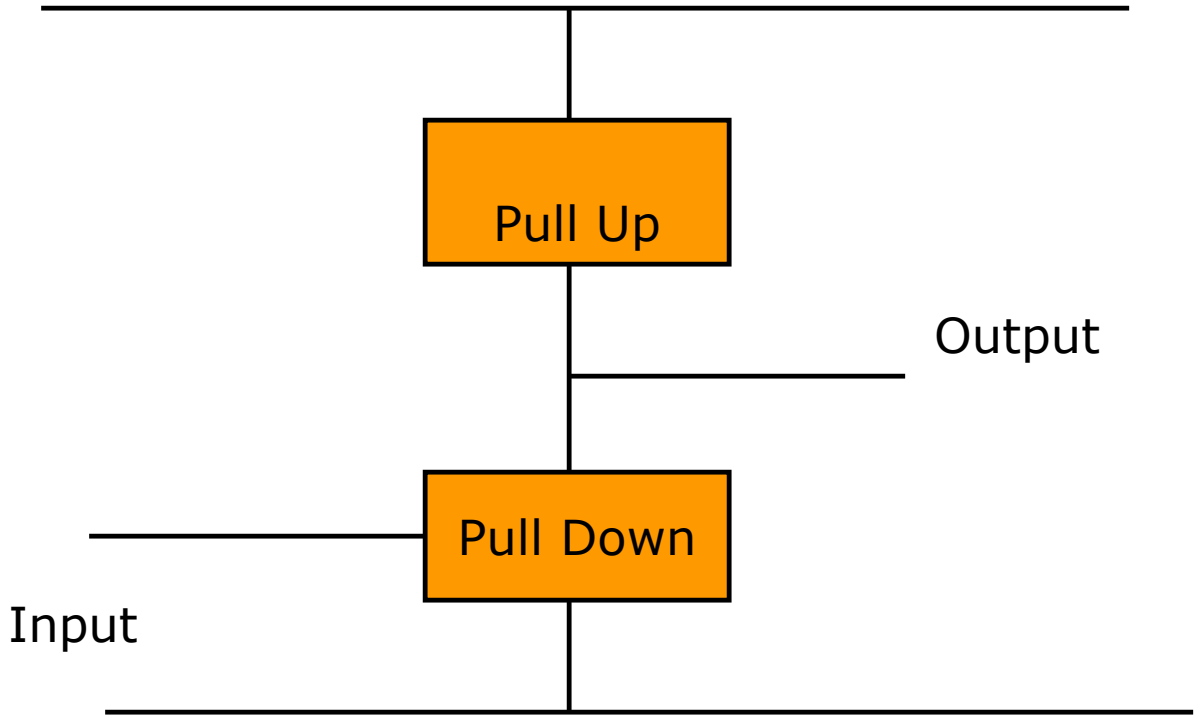
L:W

pFET/pMOS

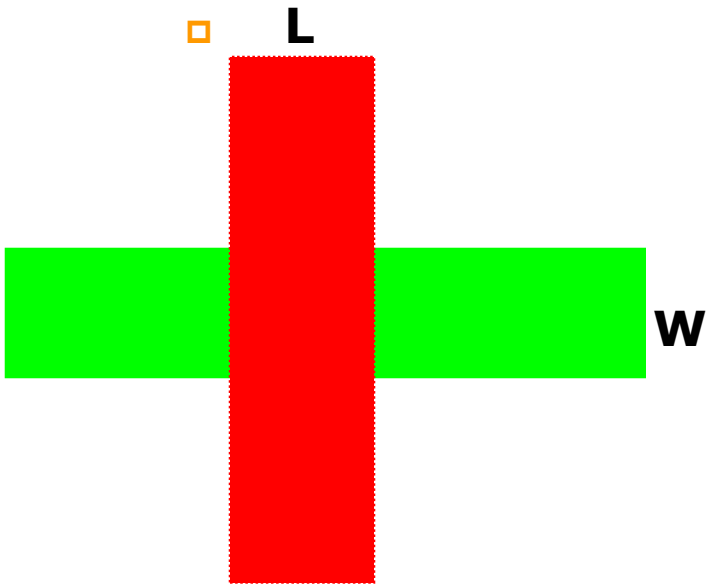
Inverter Using MOSFET

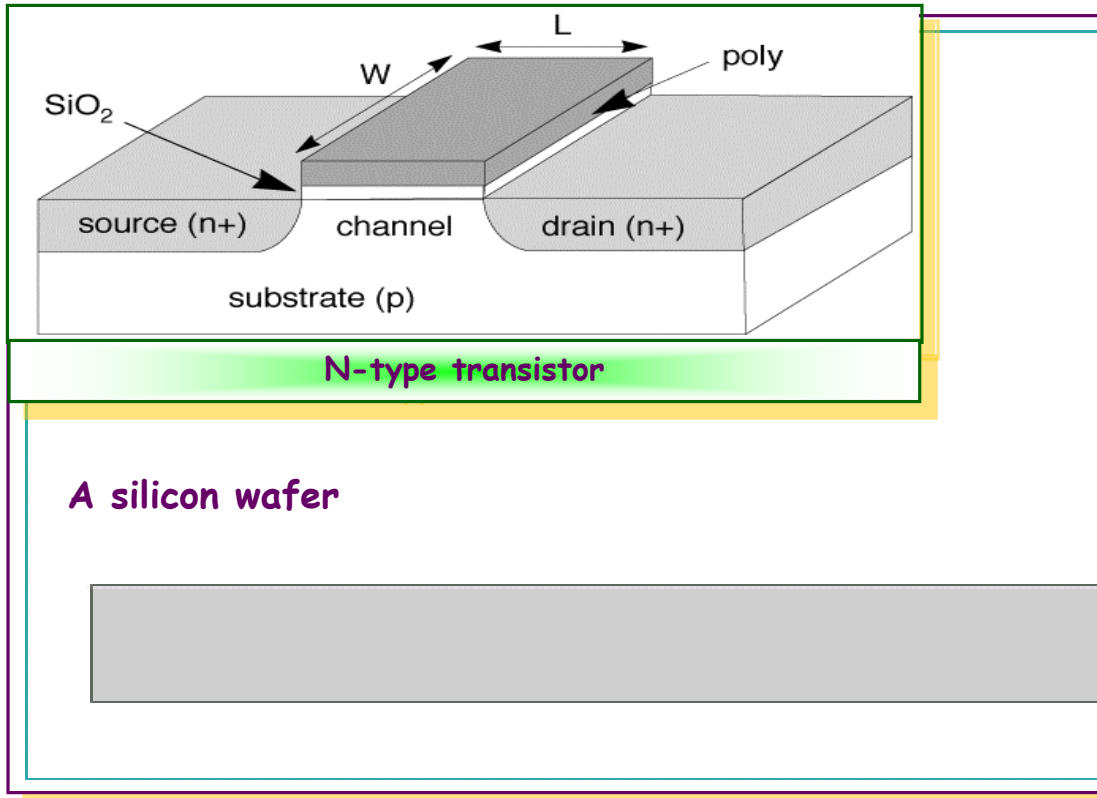
- Enhancement-Mode MOSFETs act as switches.
- They are switched OFF, when the input to gate is low.
- So, they can be used to pull the output down.
- Now, for pull-up, we can use a resistor.
- But resistors consume larger area.
- Another alternative is using MOSFET as pull-up.
- PU's can be NMOS or PMOS.

Inverter Using MOSFET



MOSFET


L
W


L
W
poly
SiO_2
source (n+)
channel
drain (n+)
substrate (p)
N-type transistor
A silicon wafer

Types of Layout Design Rules

- Industry Standard: Micron Rule
- λ Based Design Rules

Types of Design Rules (Contd…)

- Industry Standard: Micron Rule
  - All device dimensions are expressed in terms of absolute dimension(μm/nm)
  - These rules will not support proportional scaling

Types of Design Rules (Contd…)

- λ Based Design Rules :
  - Developed by Mead and Conway.
  - All device dimensions are expresses in terms of a scalable parameter λ.
  - λ = L/2; L = The minimum feature size of transistor
  - L = 2 λ
  - These rules support proportional scaling.
  - They should be applied carefully in sub-micron CMOS process.

Design Rules

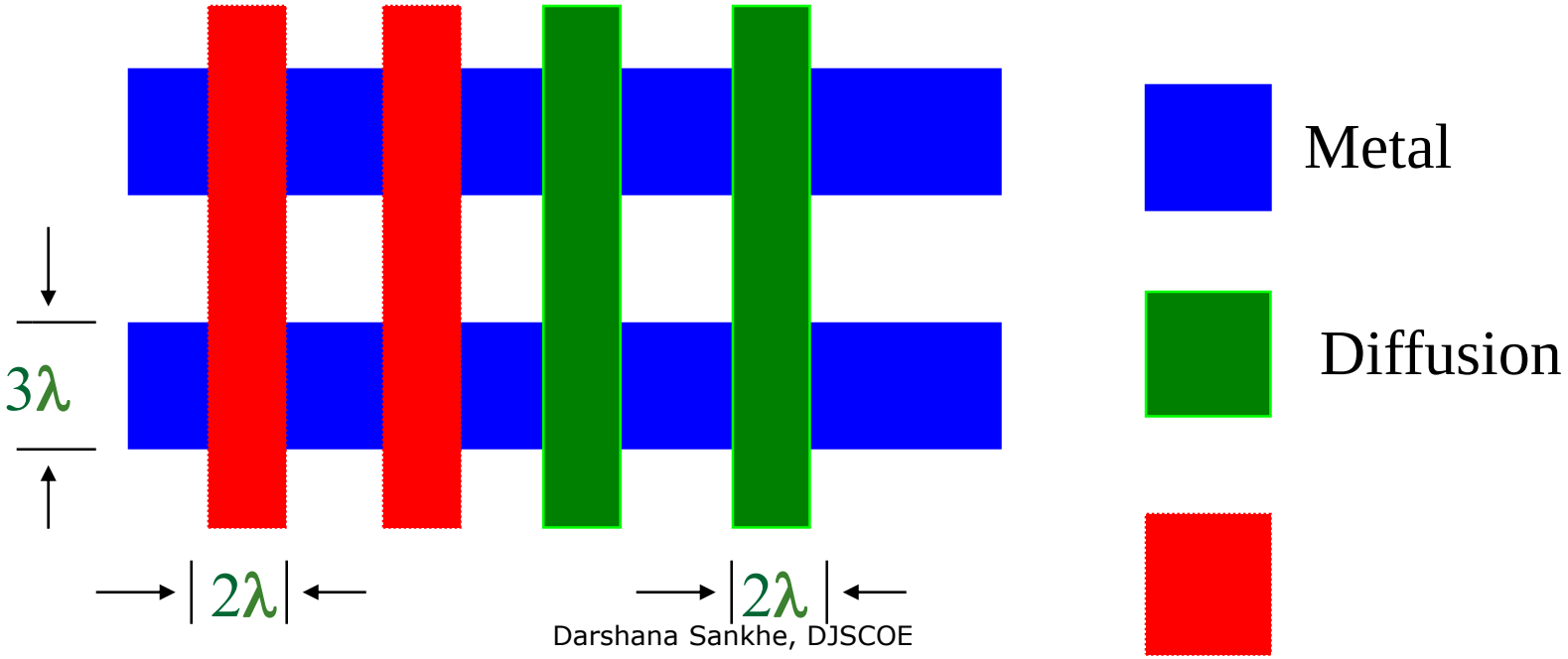
- Minimum length or width of a feature on a layer is **2λ**
  - To allow for shape contraction
- Minimum separation of features on a layer is 2λ
  - To ensure adequate continuity of the intervening materials.

Design Rules :

- Two Features on different mask layers can be misaligned by a maximum of 2λ on the wafer.
- If the overlap of these two different mask layers can be catastrophic to the design, they must be separated by at least 2λ
- If the overlap is just undesirable, they must be separated by at least λ

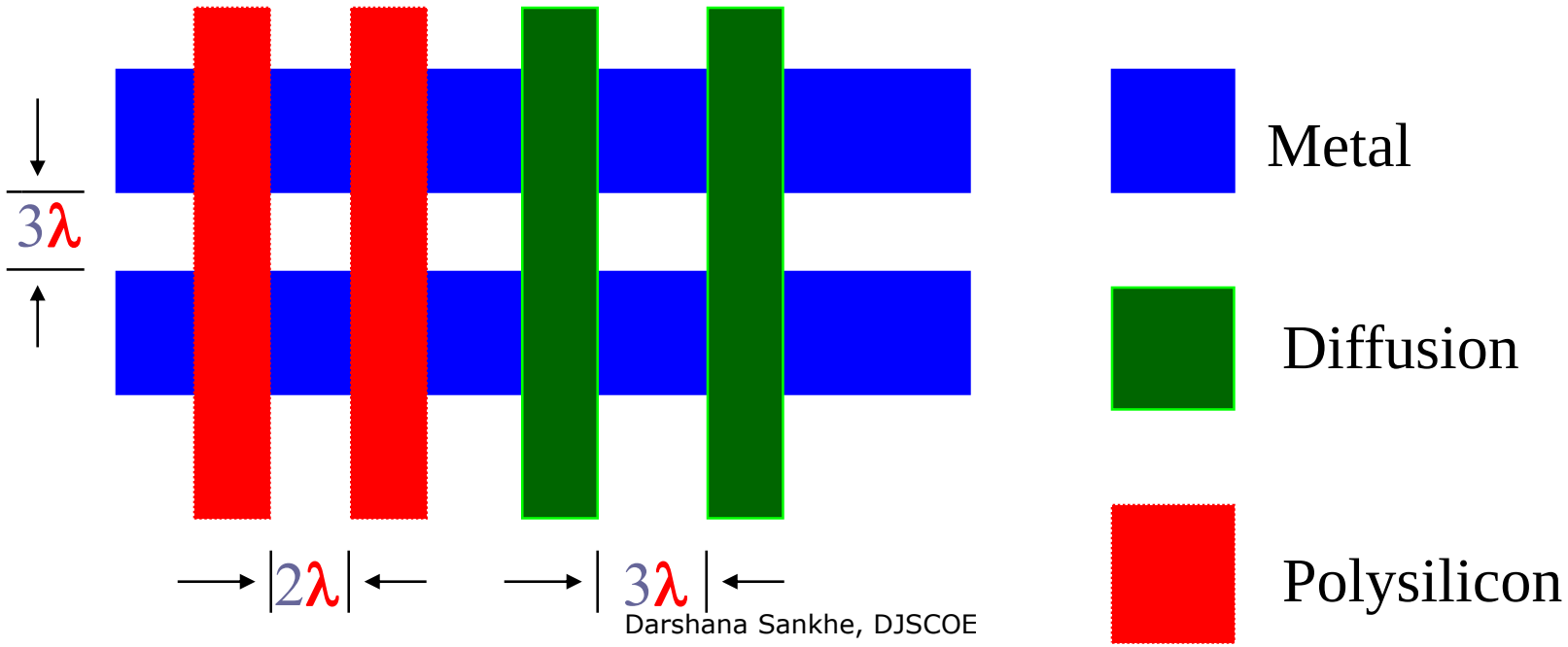
Design Rules: NMOS

- Minimum width of PolySi and diffusion line **2λ**
- Minimum width of Metal line **3λ** as metal lines run over a more uneven surface than other conducting layers to ensure their continuity



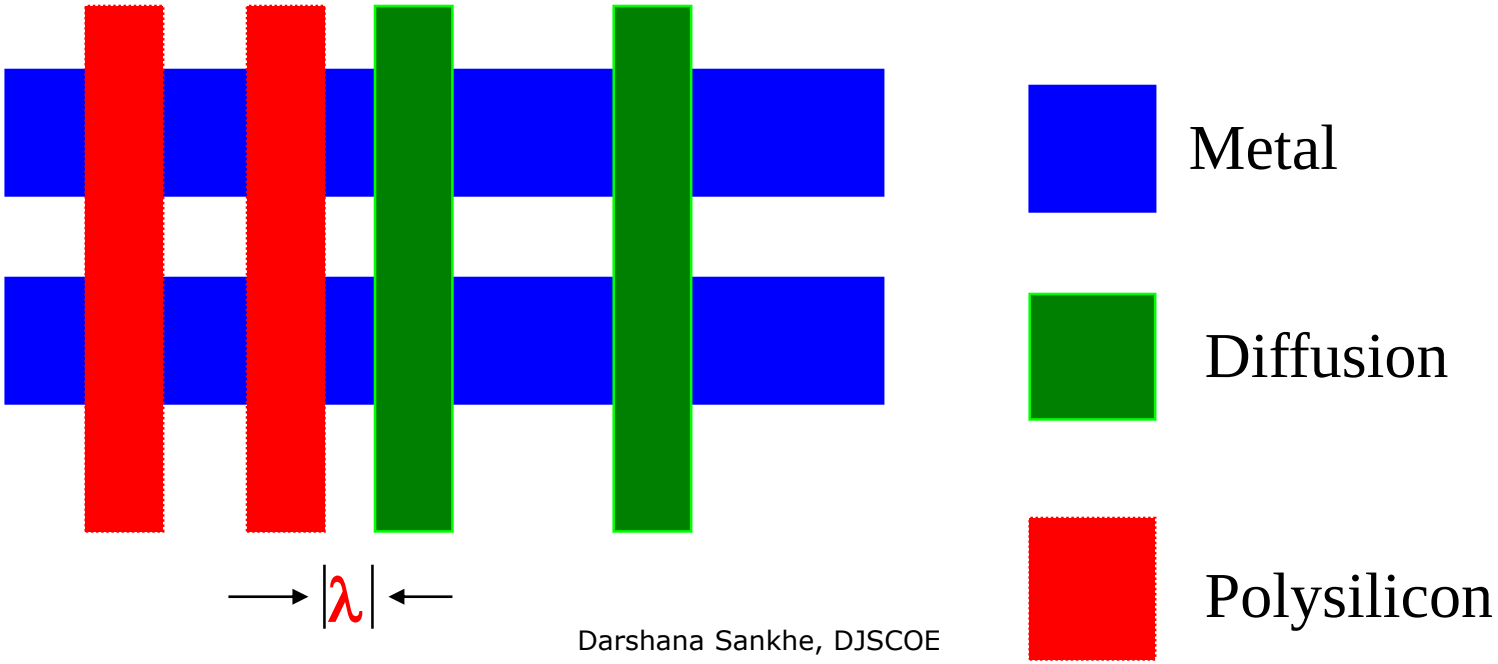
Design Rules: NMOS

- **PolySi – PolySi spacing 2λ**
- **Metal - Metal spacing 3λ**
- **Diffusion – Diffusion spacing 3λ To avoid the possibility of their associated regions overlapping and conducting current**



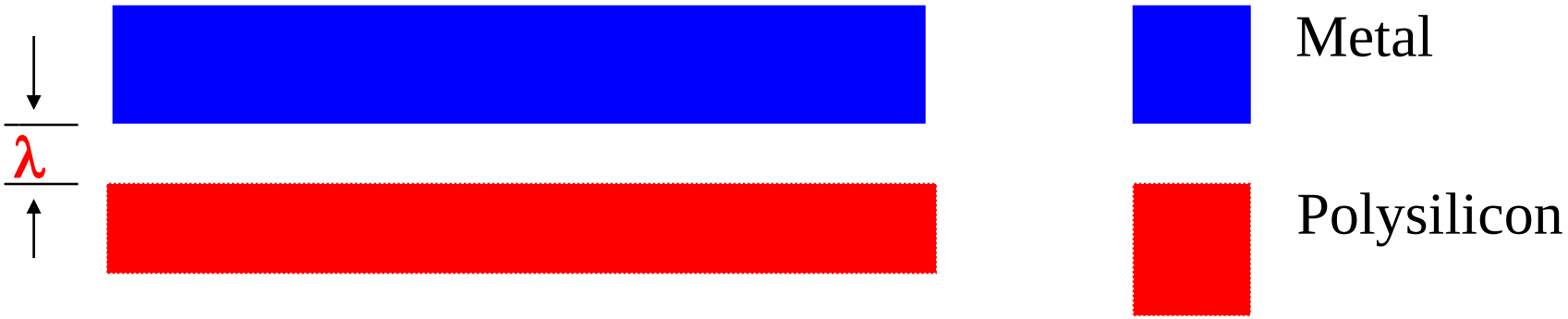
Design Rules: NMOS

- **Diffusion – PolySi spacing λ To prevent the lines overlapping to form unwanted capacitor.**
- **Metal lines can pass over both diffusion and polySi without electrical effect. Where no separation is specified, metal lines can overlap or cross.**



Design Rules: NMOS

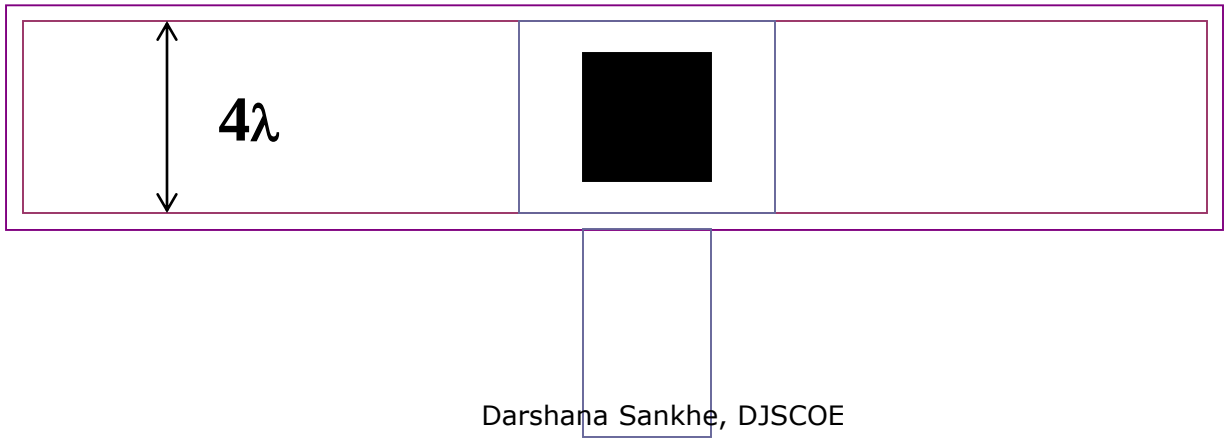
- **Metal lines can pass over both diffusion and polySi without electrical effect**
- **It is recommended practice to leave λ between a metal edge and a polySi or diffusion line to which it is not electrically connected**



Contact Cut :

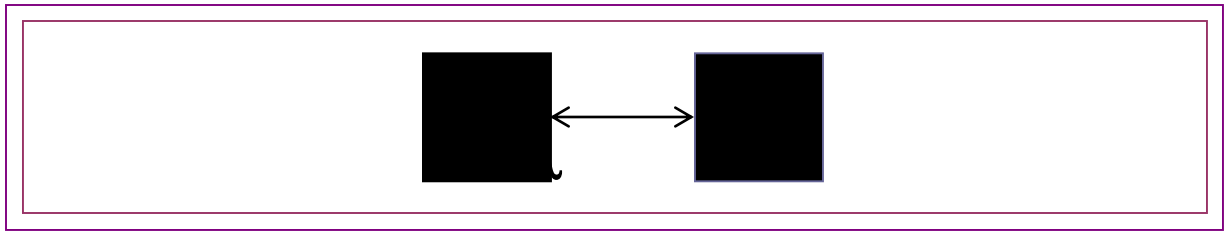
- **Metal connects to polySi/diffusion by contact cut.**
- **Contact area: 2λ*2λ**

- **Metal and polySi or diffusion must overlap this contact area by λ so that the two desired conductors encompass the contact area despite any mis-alignment between conducting layers and the contact hole**



Contact Cut

- **Contact cut – contact cut: 2λ apart**
- **Why? To prevent holes from merging.**



Design Rules: NMOS

- Minimum diff width 2λ
- Minimum poly width 2λ
- Minimum metal width 3λ
- poly-poly spacing 2λ

- diff-diff spacing 3λ

  (depletion regions tend to spread outward)
- metal-metal spacing 3λ

- diff-poly spacing λ

Design Rules: NMOS

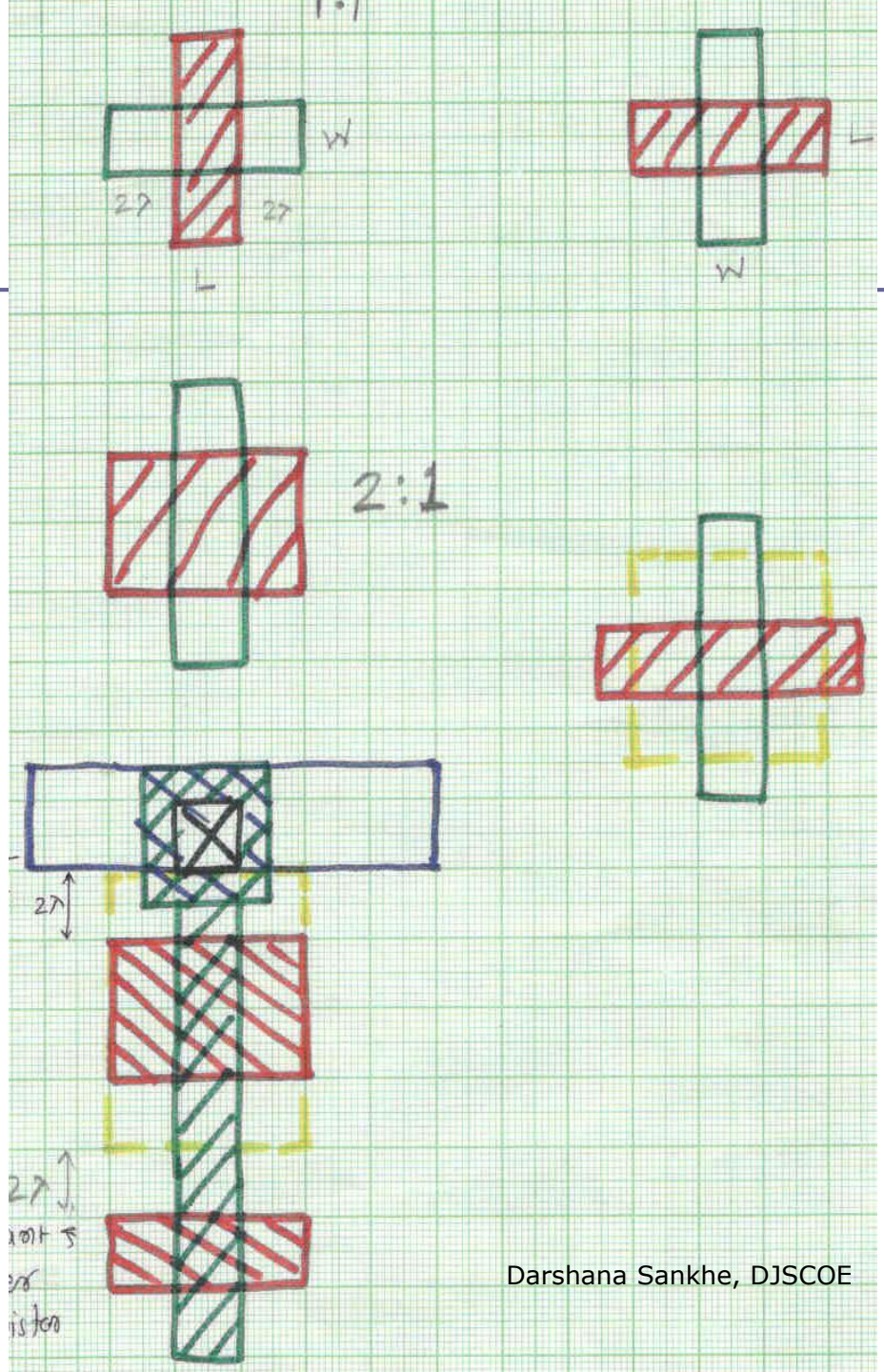
- Poly gate extend beyond diff by 2λ
- Diff extend beyond poly by 2λ
- Contact size 2λ * 2λ
- Contact diff/poly/metal overlap 1λ
- Contact to contact spacing 2λ
- Contact to poly/diff spacing 2λ
- Buried contact to active device spacing 2λ
- Buried contact overlap in diff direction 2λ
- Buried contact overlap in poly direction 1λ
- Implant gate overlap 2λ

Aspect Ratio For Pull-up and Pull-down

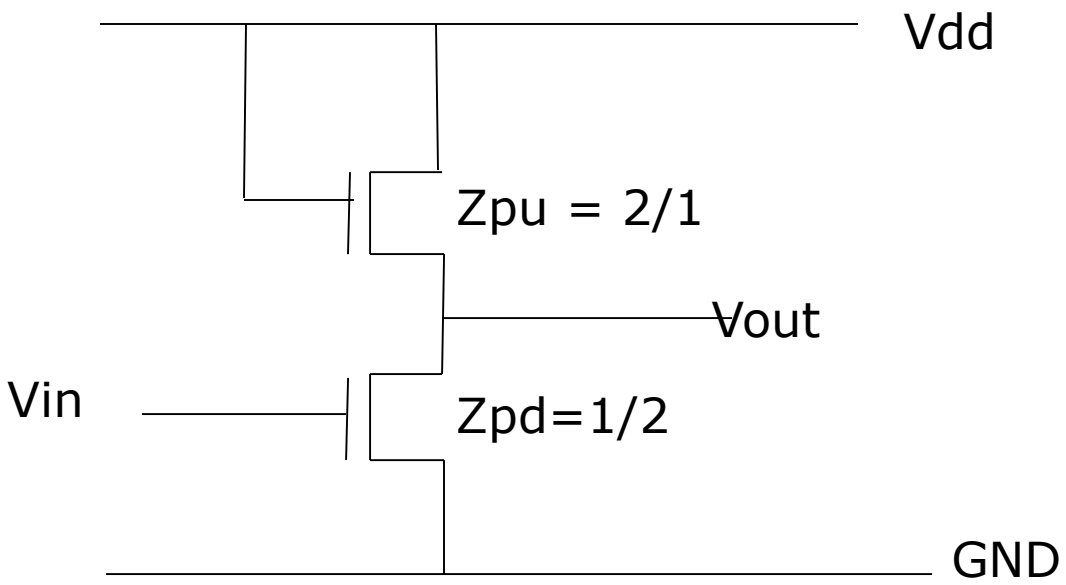
- The size of a MOSFET depends on the reference inverter design.
- The reference inverter for nMOS logic design is the inverter with depletion mode load.
- Z_{PD} = Aspect Ratio of pull-down= L_{PD}/W_{PD}
- Z_{PU} = Aspect Ratio of pull-up= L_{PU}/W_{PU}
- The ratio of aspect ratio of Pull-up and Pull-down is known as Inverter Ratio i.e. $R_{inv} = Z_{PU} / Z_{PD}$
- When we draw a stick diagram, inverter ratio should be mentioned for that gate.
- When a we draw a stick diagram, aspect ratio should be mentioned for all the MOSFETS.

Inverter Ratio for NMOS Gates :

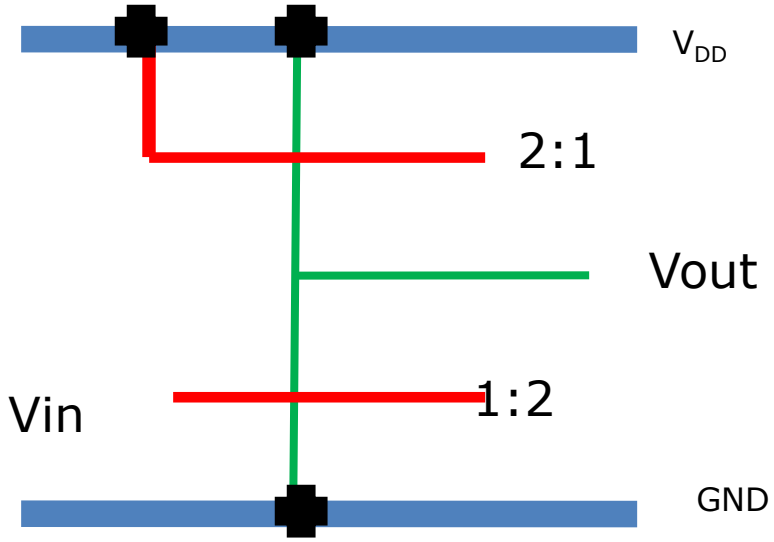
Gates	R_{inv}	Z_{PU}	Z_{PD}
Inverter	4	2:1	1:2
		4:1	1:1
	8	8:1	1:1
		4:1	1:2
		2:1	1:4
NAND (2 I/P)	4	4:1	1:2 (Each)
		2:1	1:4 (Each)
NOR (2 I/P)	4	2:1	1:2 (Each)
		4:1	1:1 (Each)


1:1
W
L
2:1
2T
2T

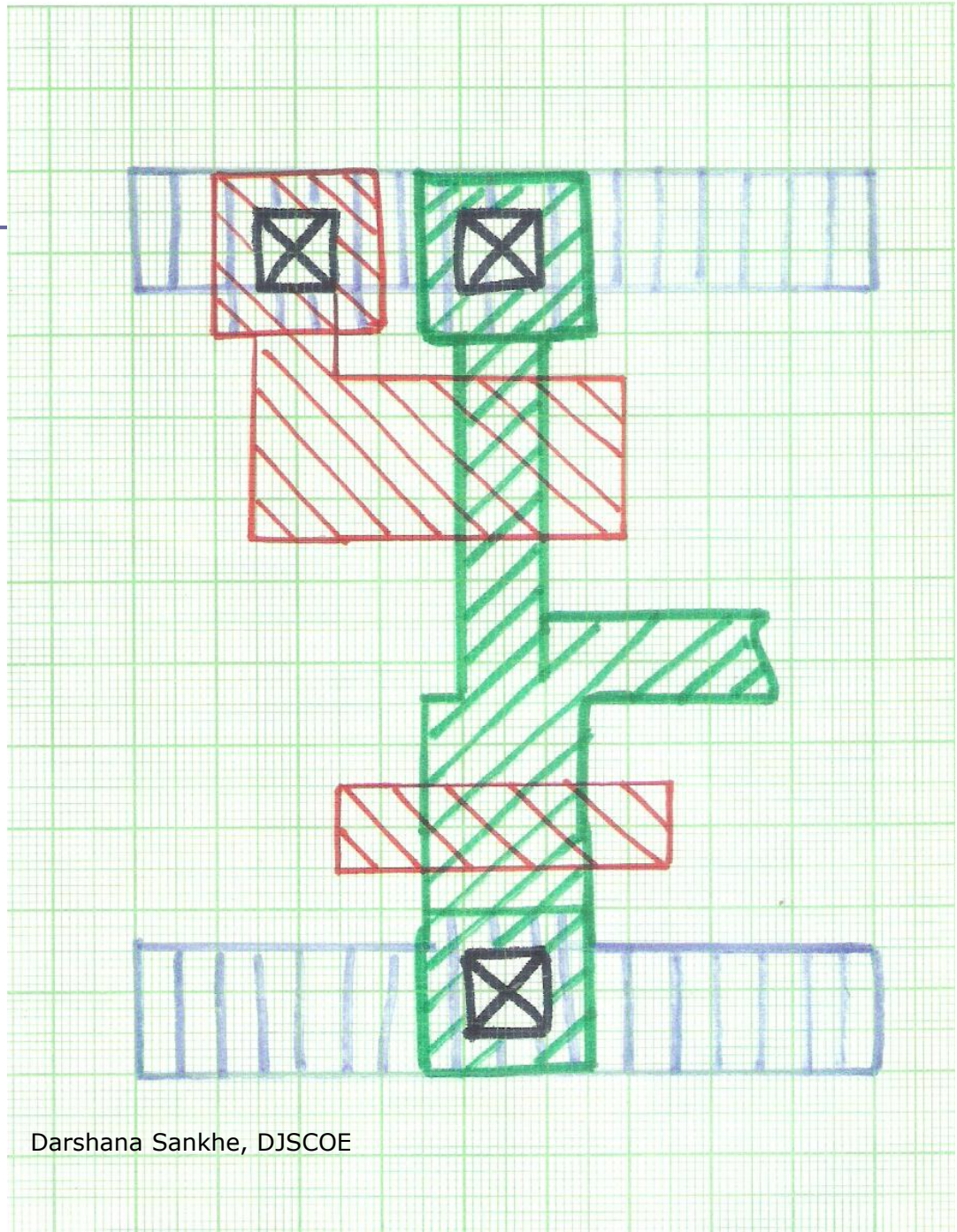
NMOS Inverter: Enhancement load



NMOS Inverter: Enhancement load (Stick diagram)



NMOS INVERTER- Enhancement load



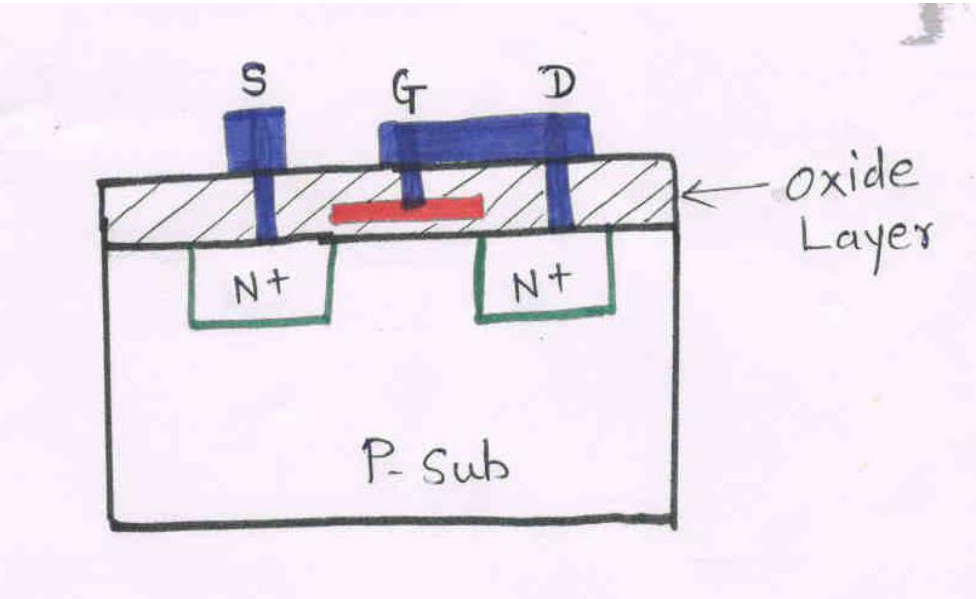
Interlayer Contacts :

- Interconnection between poly and diffusion is done by contacts.

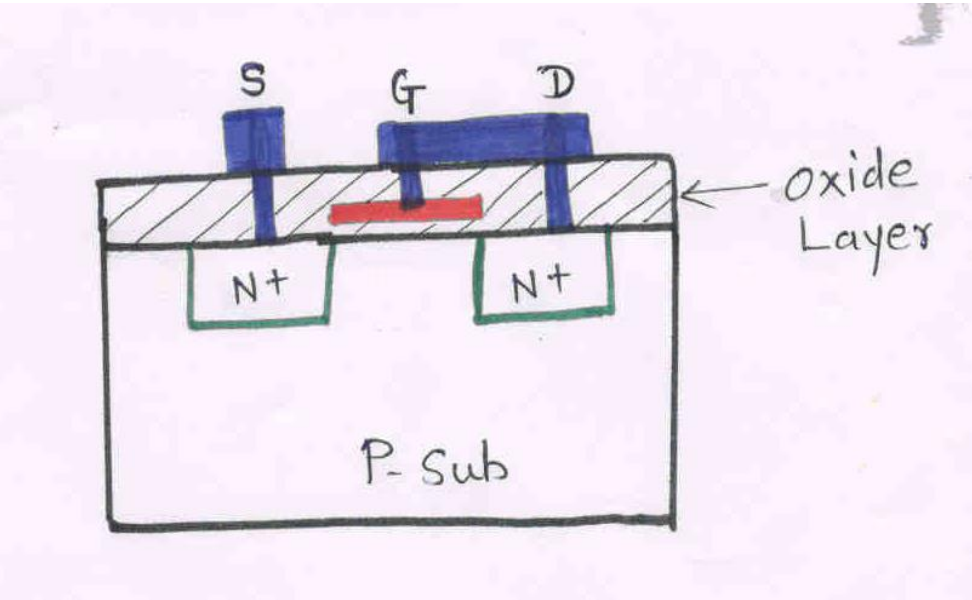
- Metal contact
- Butting contact
- Buried contact

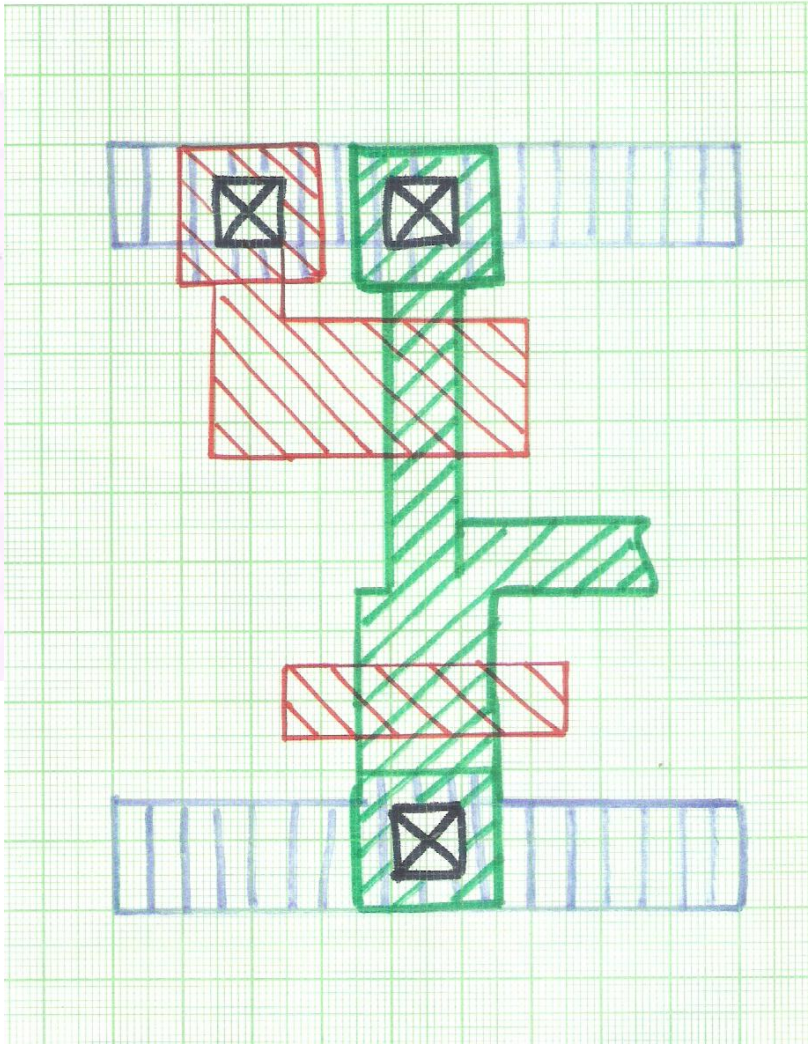
Metal contact :

- Contact cut of 2λ * 2λ in oxide layer above poly and diffusion
- Metal used for interconnection
- Individual contact size becomes 4λ * 4λ



Metal contact :





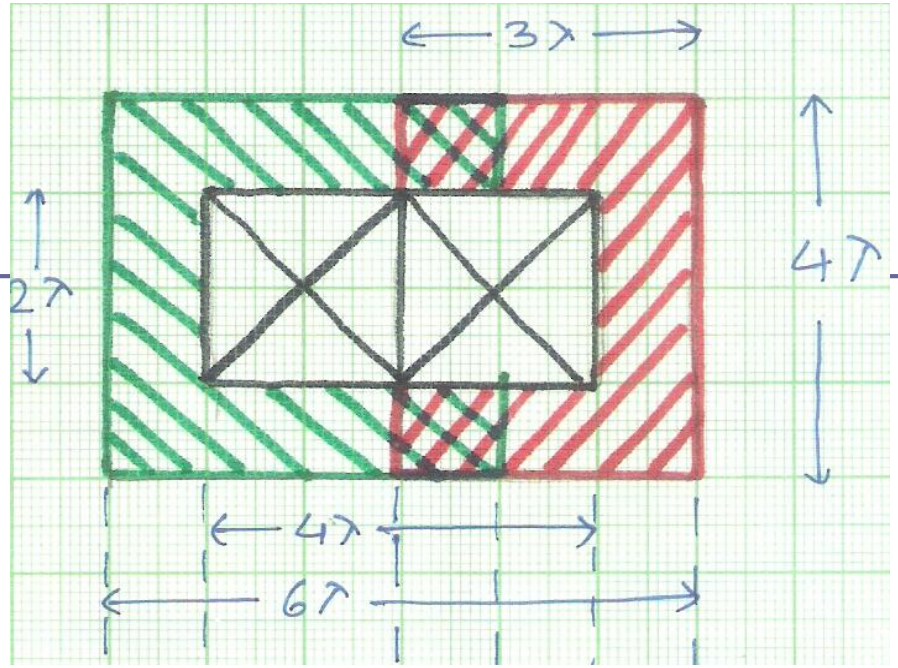
Butting Contact

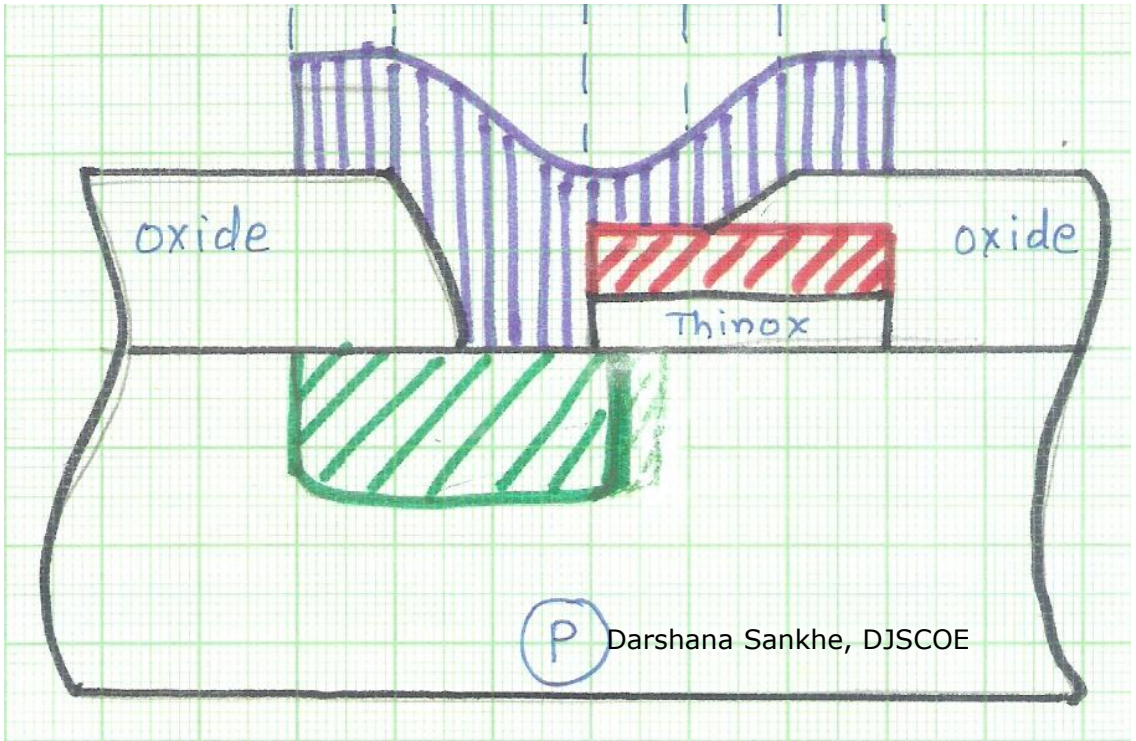
- The Poly(gate) and diffusion(Drain) of NMOS device can be connected by a **butting contact.**

- **Two contact cuts are adjacent to each other**
- **Therefore effective contact area is less**

- Here metal makes contact to both the diffusion forming the drain of the transistor and to the polySi forming this device's gate.

Butting Contact :





Butting Contact

- Metallization is required only over the butting contact holes which are 2 λ x 4λ in size
- A border of width λ around all four sides is added to allow for mis-registration and to ensure proper contact.
- This brings the metallization size to 4λ x6λ

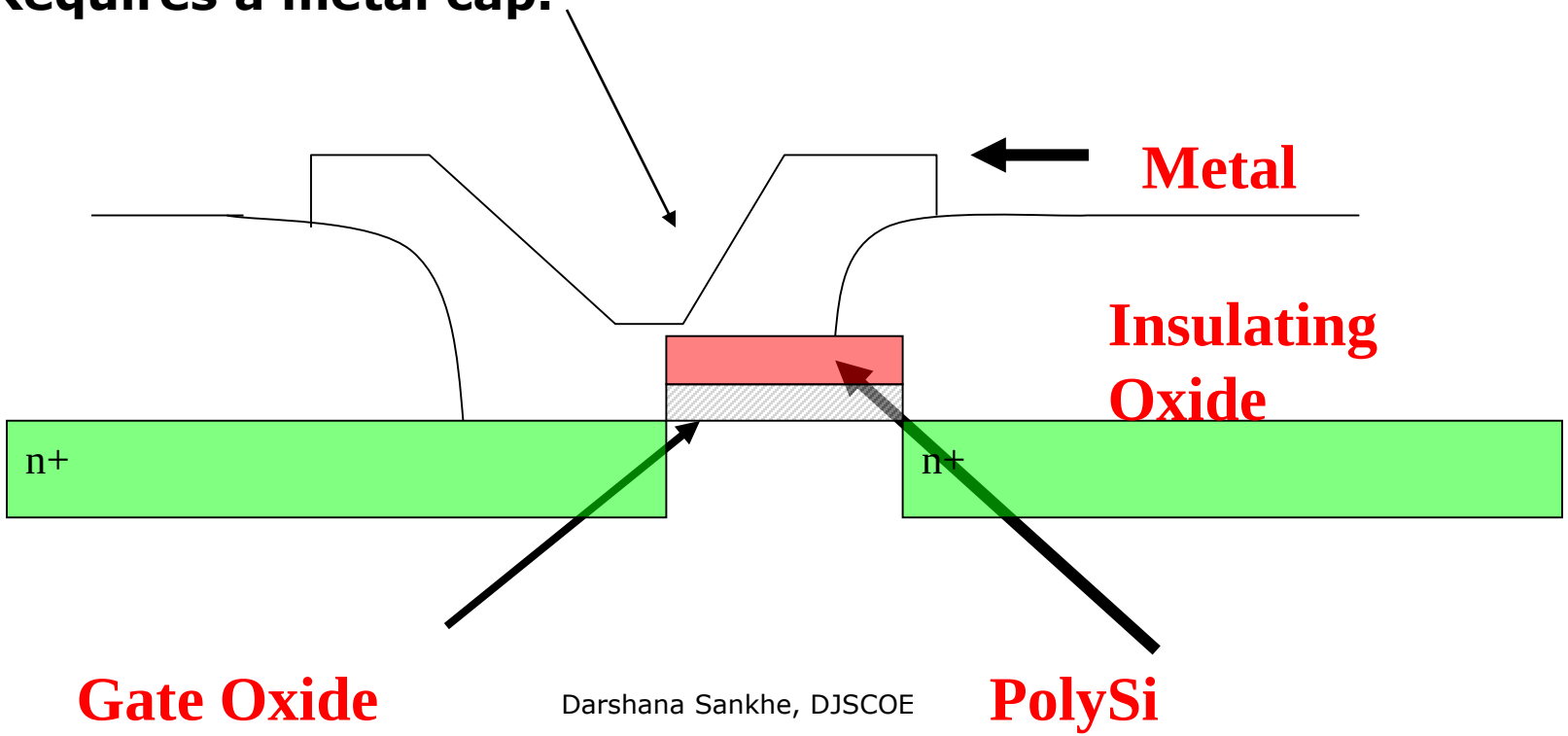
Advantage:

- No buried contact mask required and avoids associated processing.

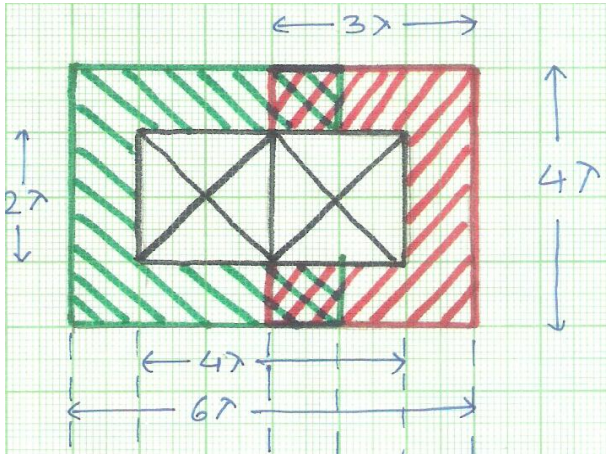
Butting Contact

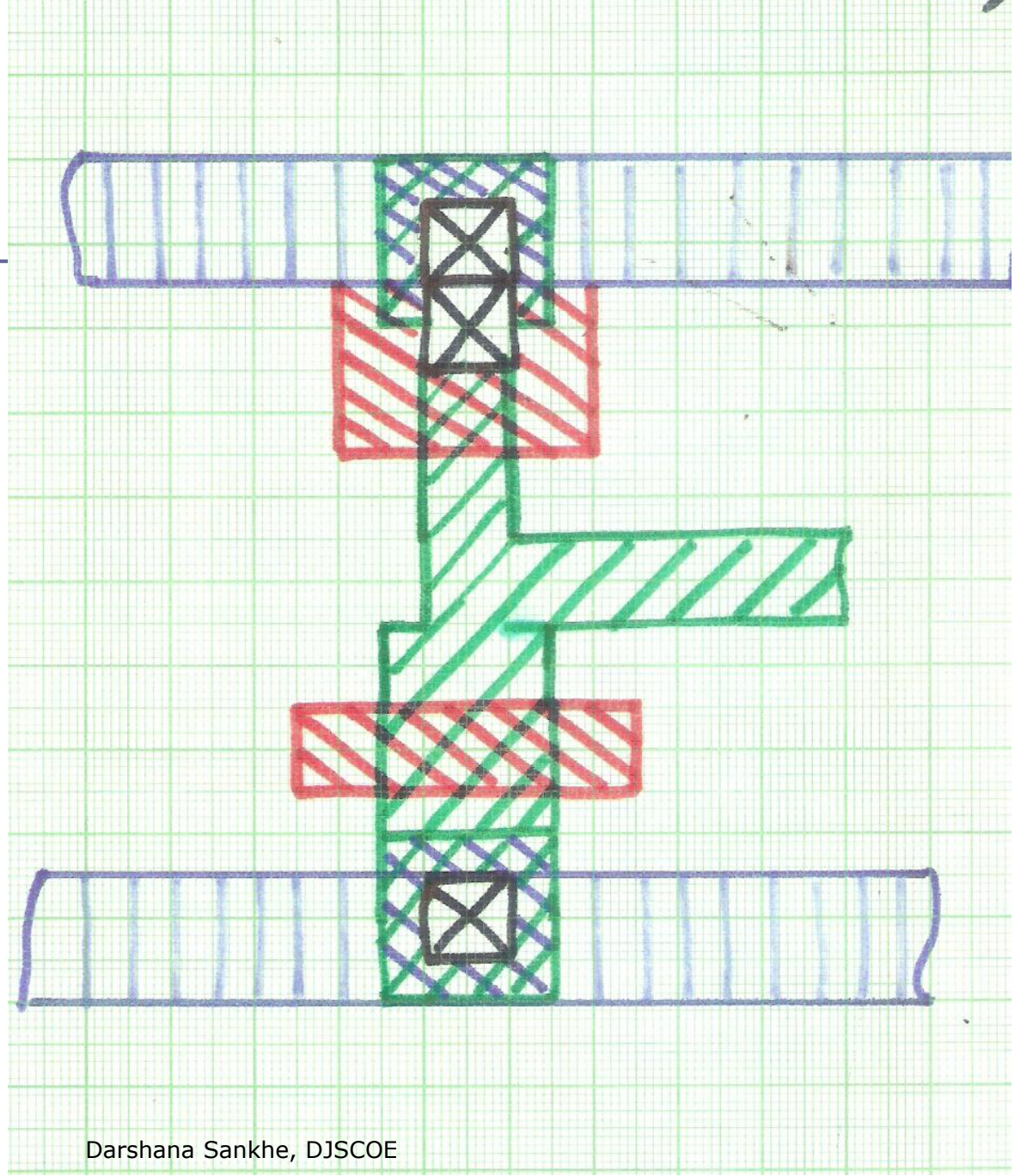
Disadvantages:

- **Metal descending the hole has a tendency to fracture at the polySi corner, causing an open circuit.**
- **Requires a metal cap.**

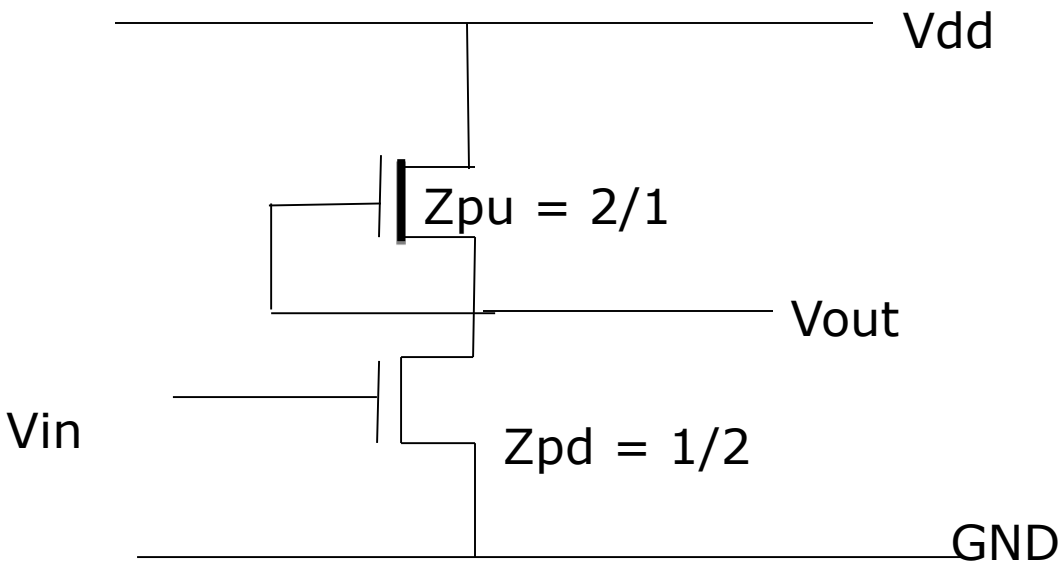


NMOS INVERTER- Enhancement load

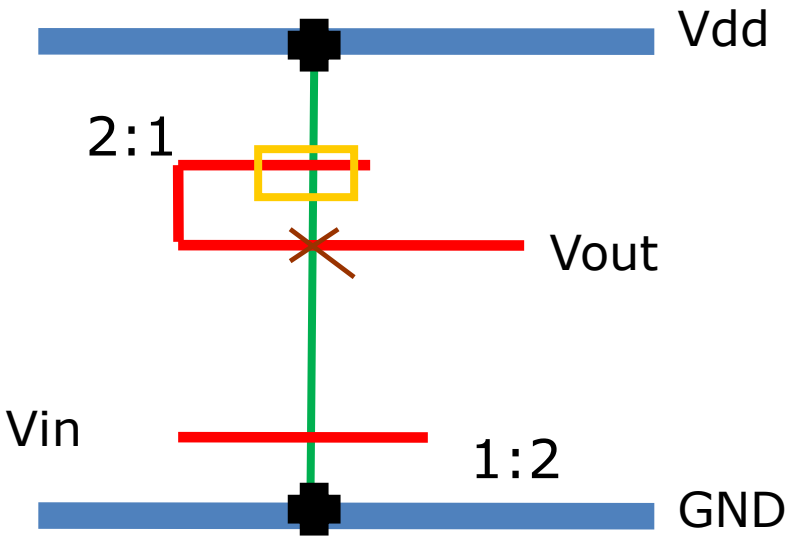




NMOS Inverter: Depletion load

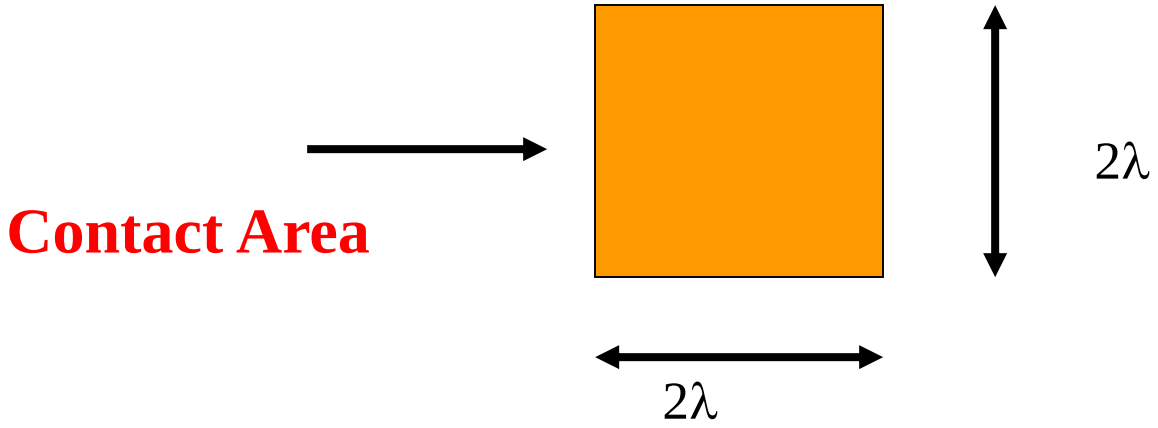


NMOS Inverter: Depletion load (Stick Diagram)



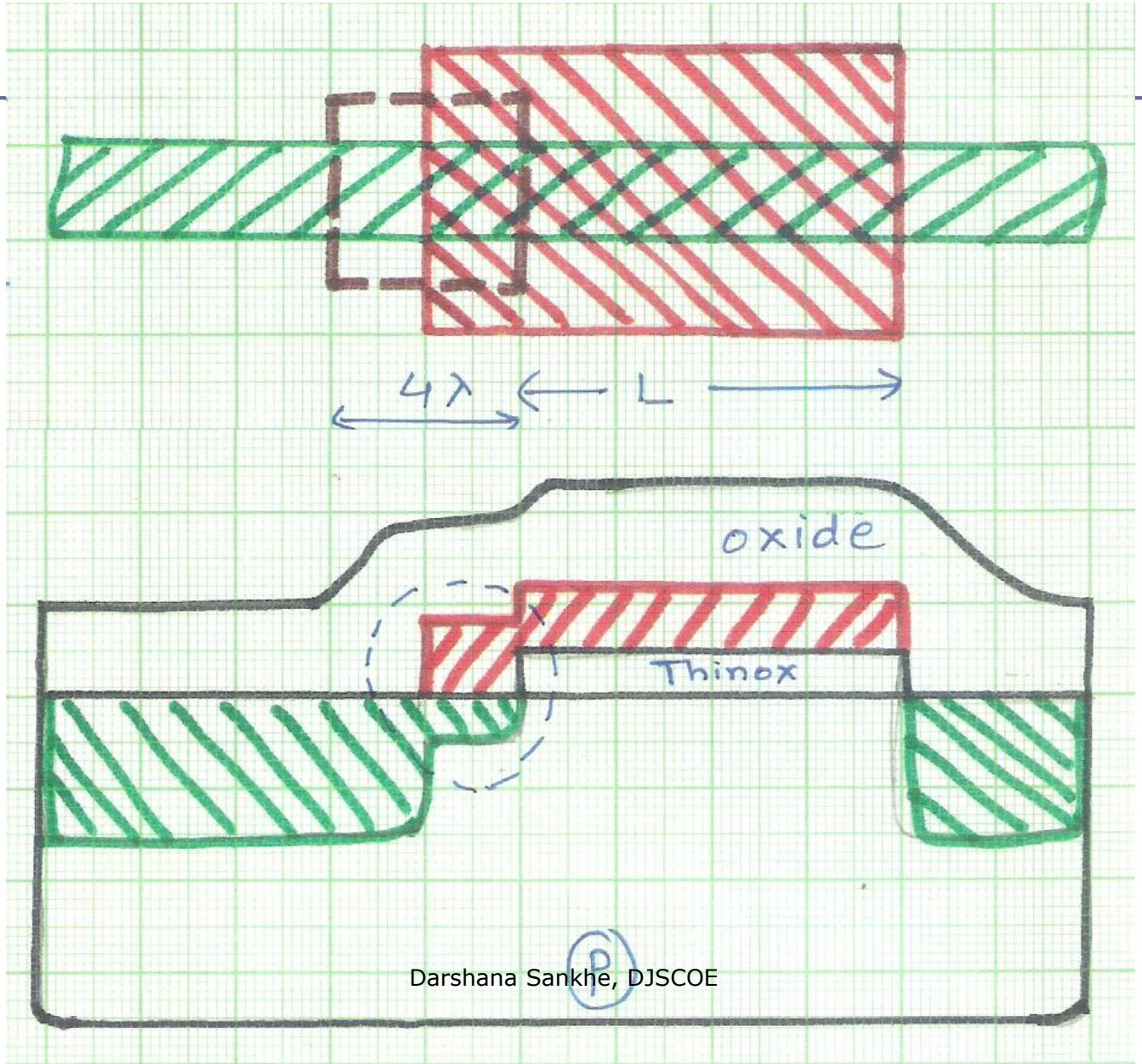
Buried Contact

- The buried contact window defines the area where oxide is to be removed so that polySi connects directly to diffusion.
- Contact Area must be a min. of 2 λ *2λ to ensure adequate contact area.

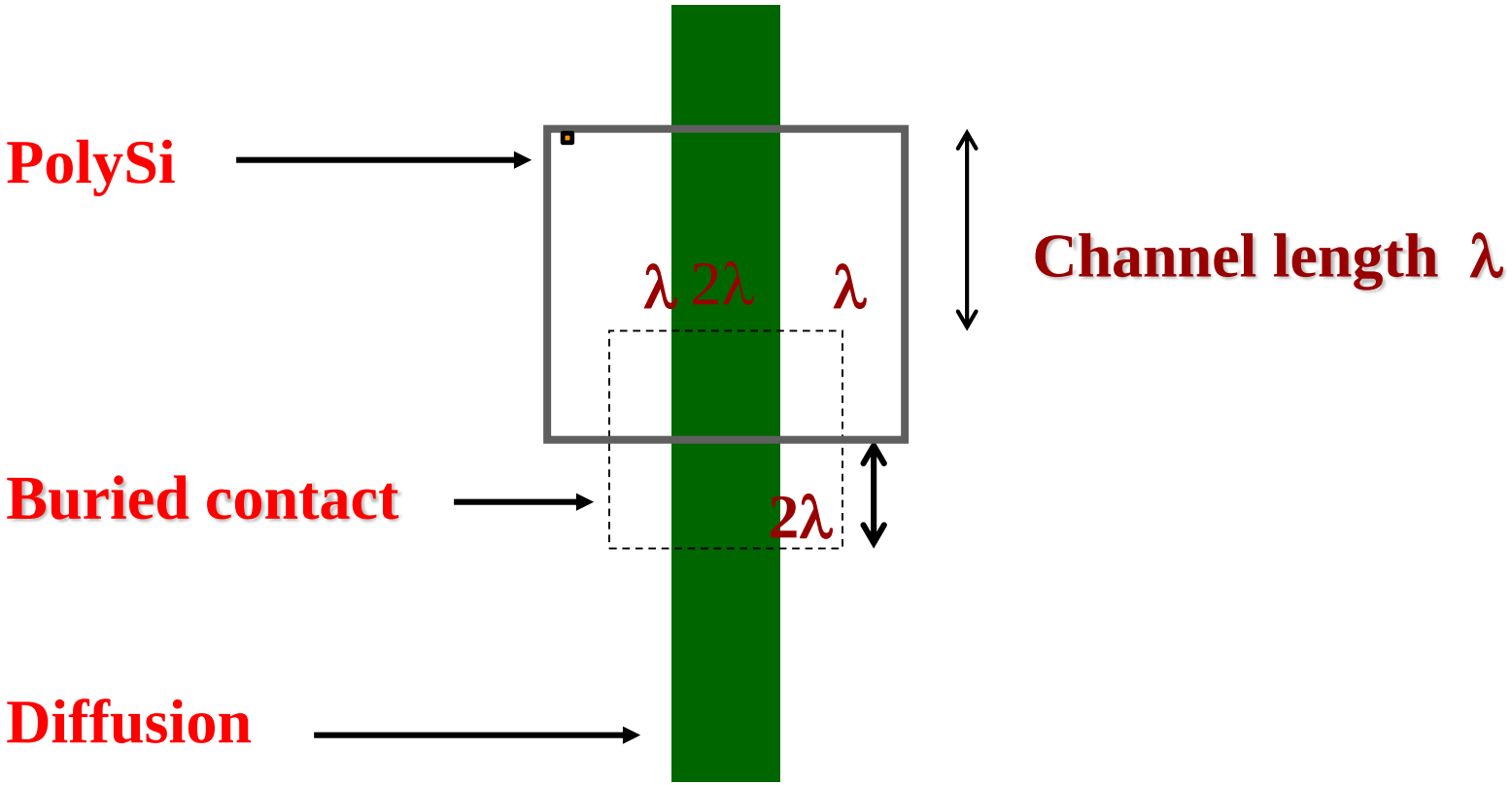


- Advantages: No metal cap required.
- Disadvantage: An extra mask is required.

Buried contact :



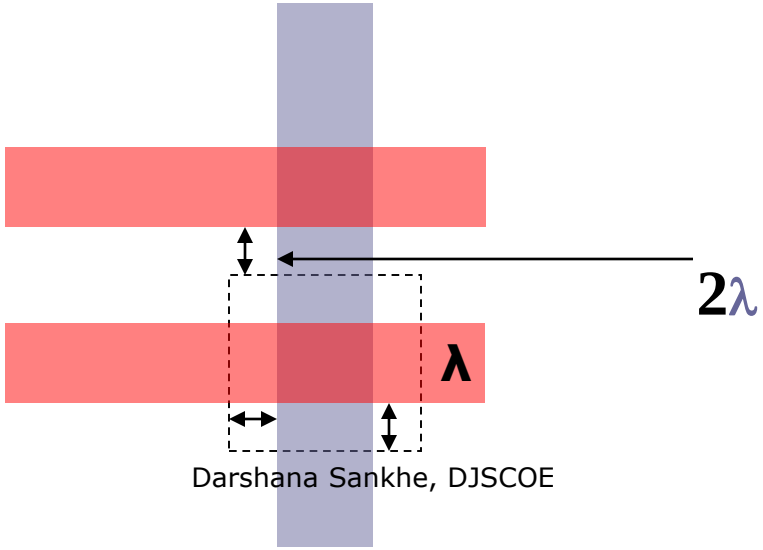
Buried Contact



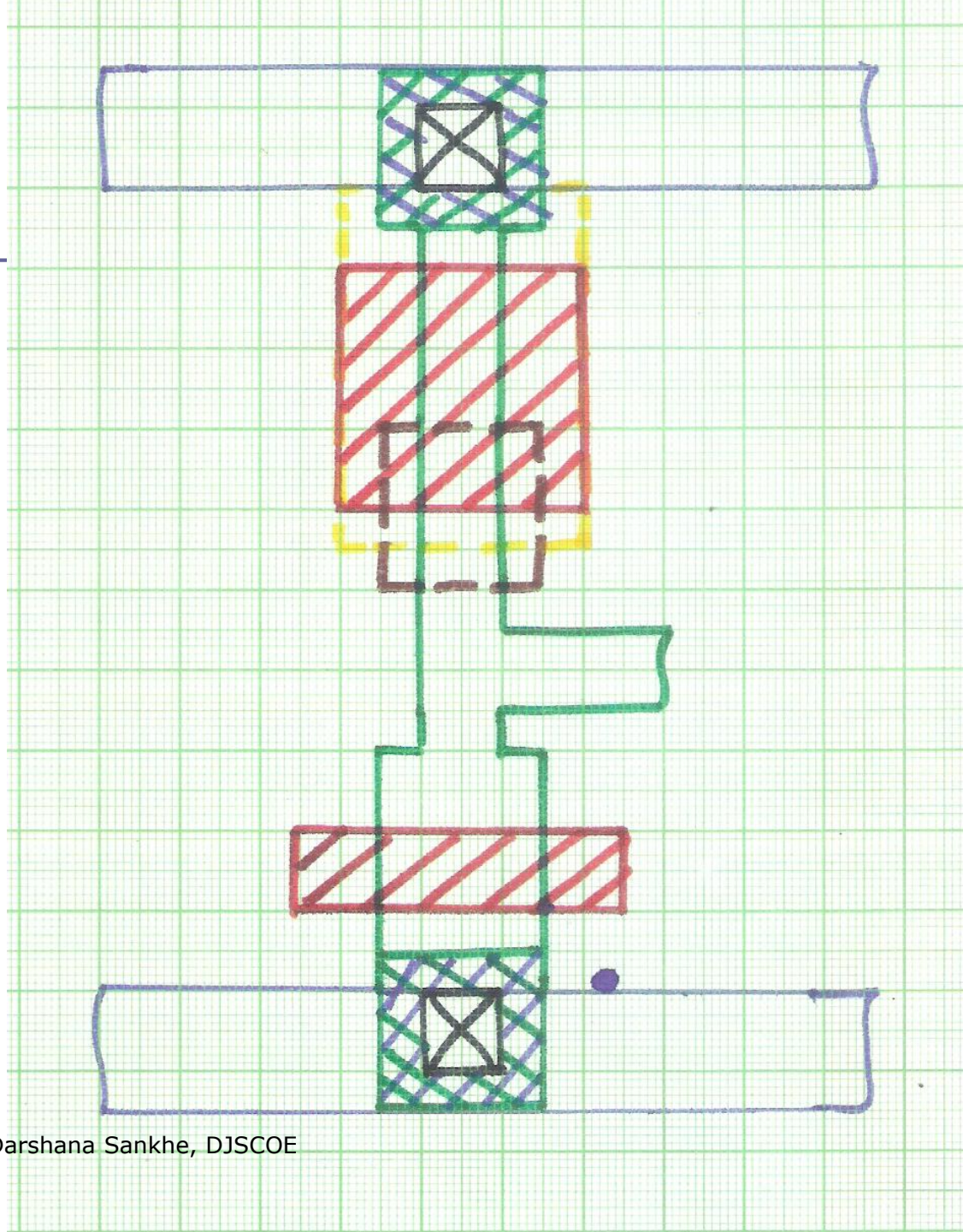
Buried Contact

- The buried contact window surrounds this contact by λ in all directions to avoid any part of this area forming a transistor.

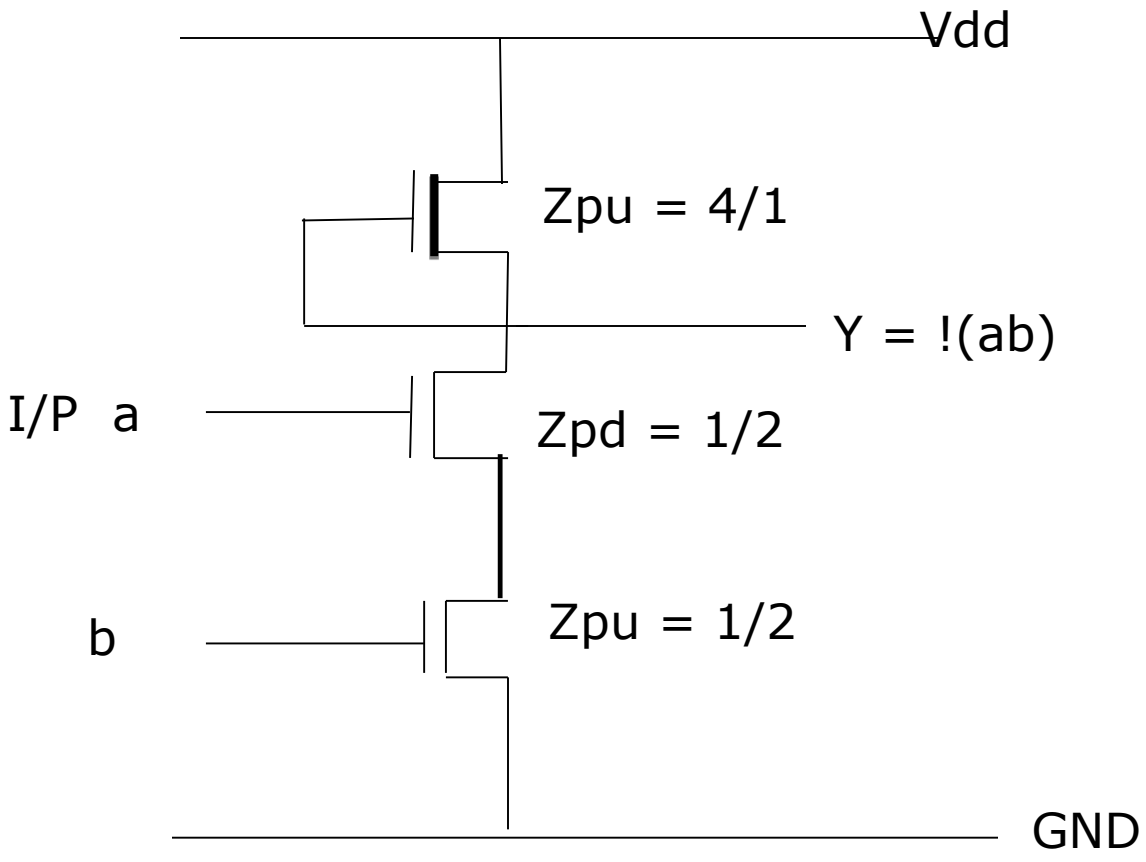
- Separated from its related transistor gate by 2λ to prevent gate area from being reduced.



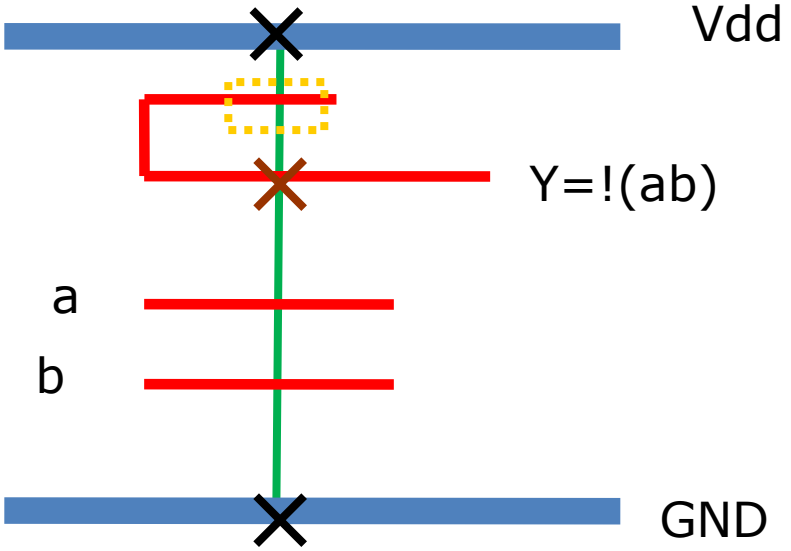
NMOS INVERTER
Depletion load



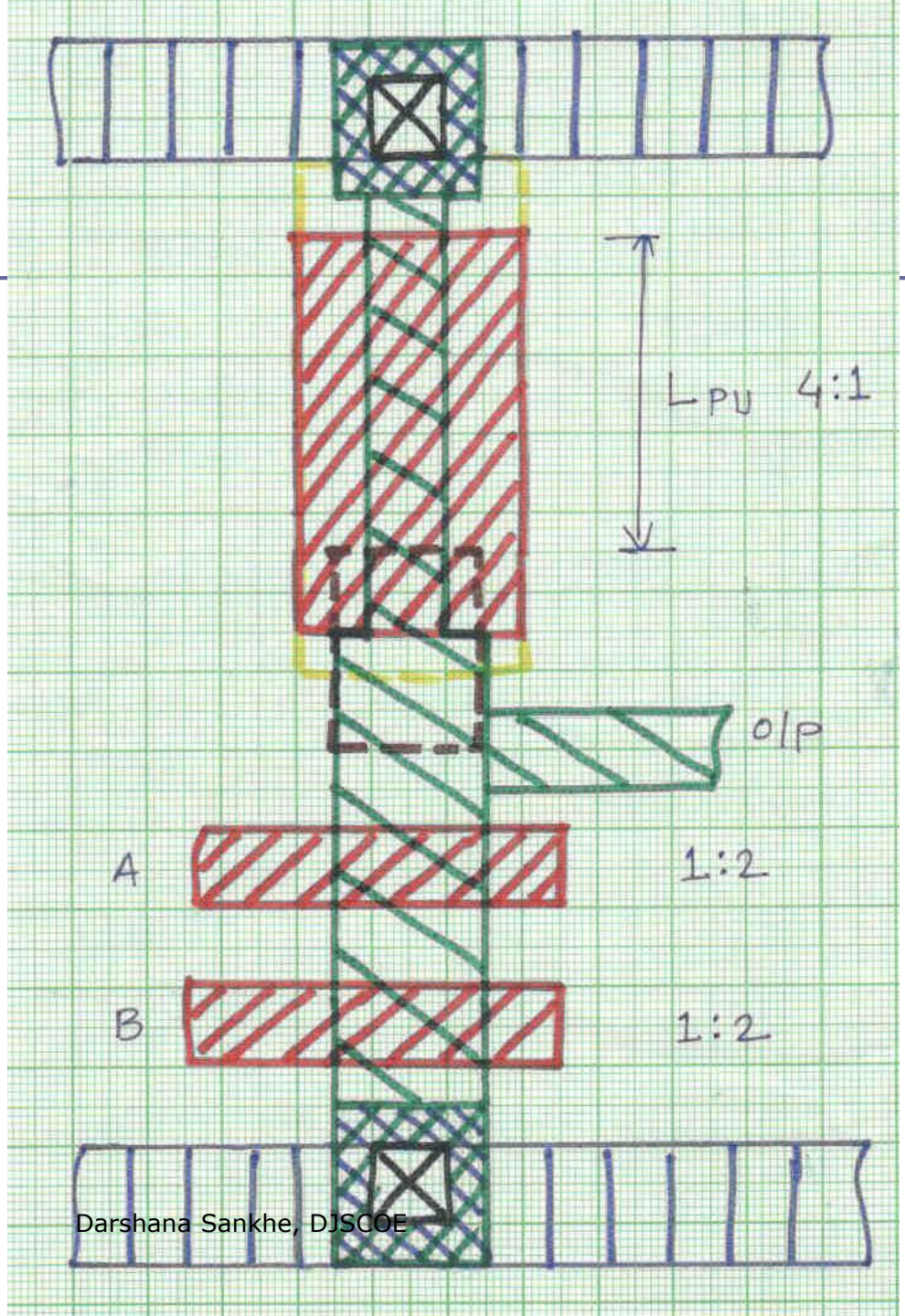
NMOS 2 I/P NAND Gate :



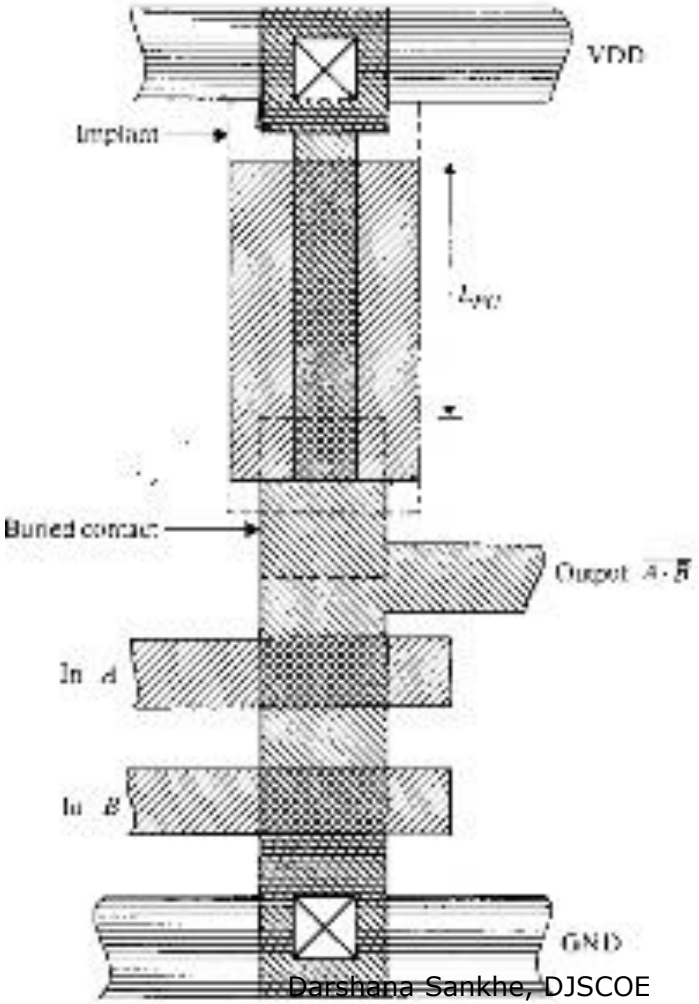
NMOS NAND (Stick Diagram) :



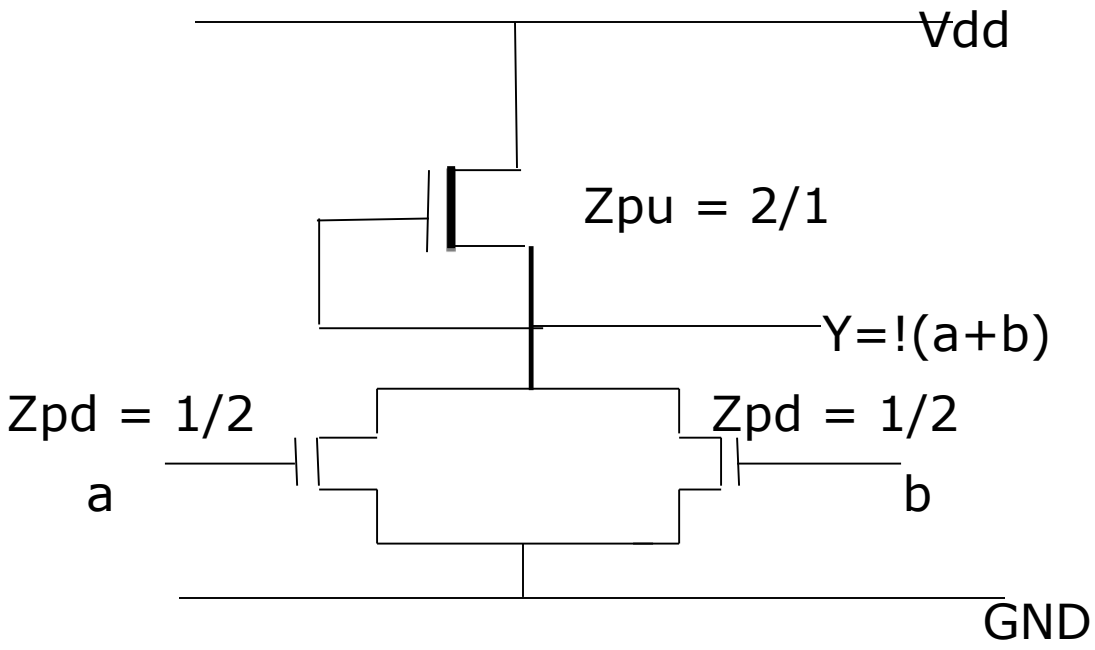
NMOS NAND



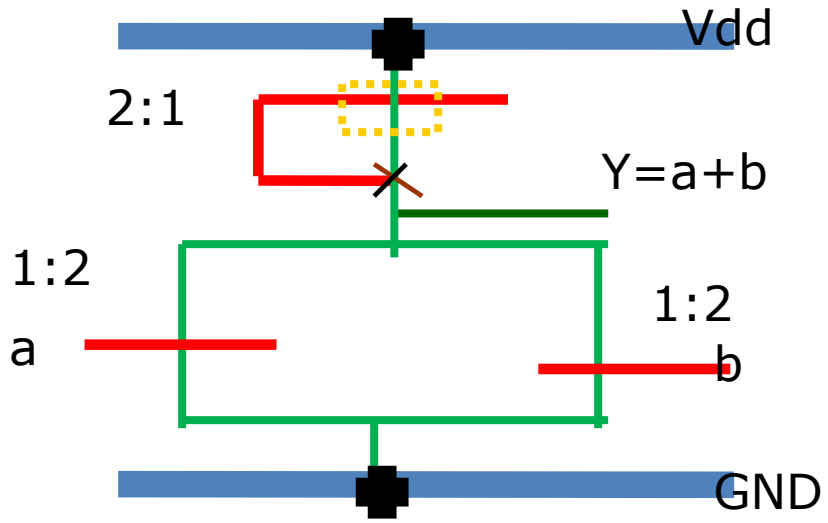
NMOS NAND


VDD
Implant
Buried contact
Output $\overline{A \cdot B}$
In A
In B
GND

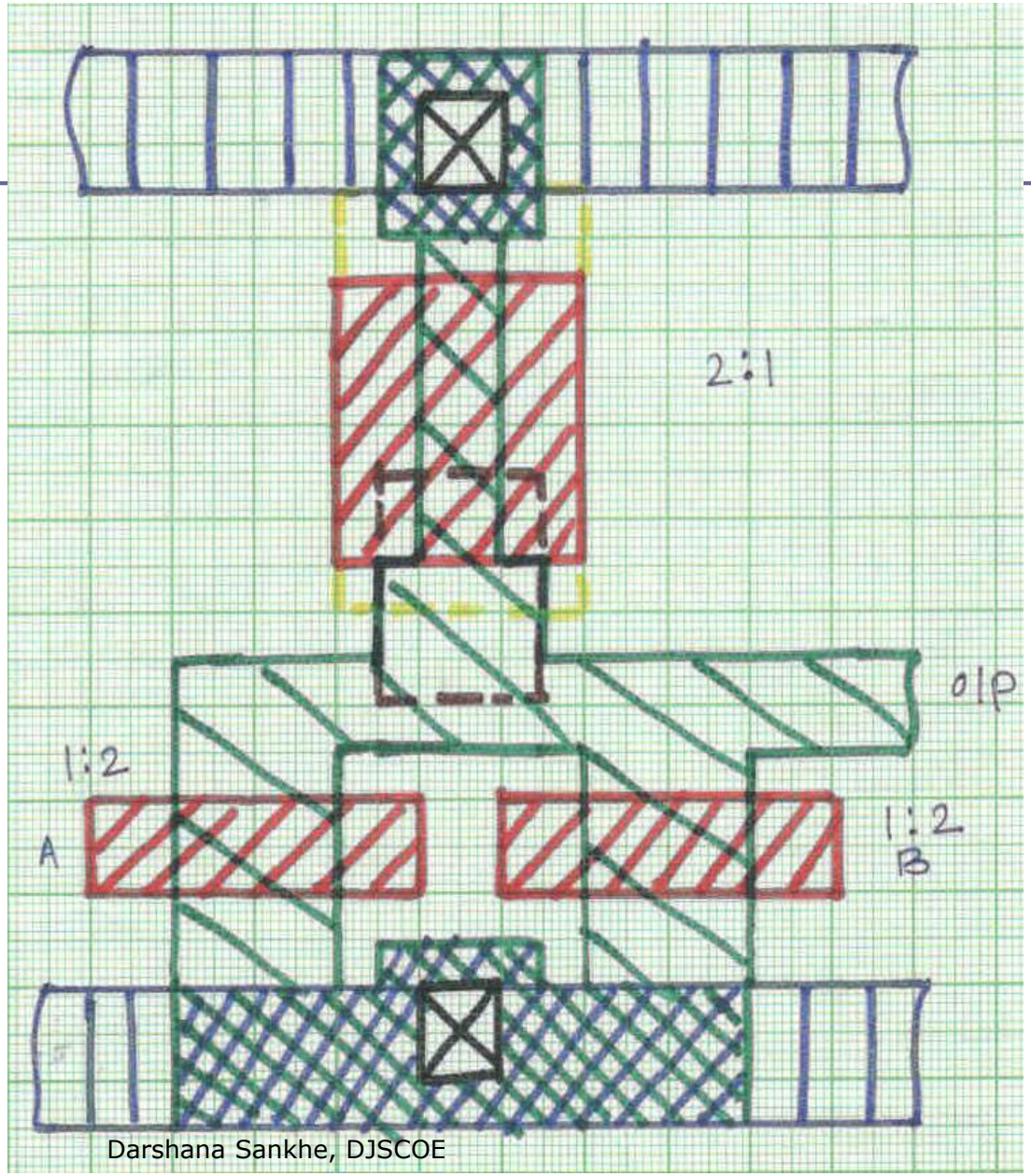
NMOS 2 I/P NOR Gate :



NMOS NOR (Stick Diagram)



NMOS NOR



NMOS NAND and NOR :

NMOS NAND

- Two nmos in series.
- Gate delay and area increases with increase in no of inputs.
- Length also increases with increase in no of input.
- NMOS NAND is slower for same no of inputs and power dissipation.

NMOS NOR

- Two nmos in parallel.
- NOR works quite well for any no of inputs.
- Width is proportional to number of inputs.
- NMOS NOR is faster for same no of inputs and power dissipation.

Thank you