POWER DISSIPATION IN CMOS CIRCUITS

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- Power Dissipation:

Power dissipation in CMOS circuits :

1. Static Power dissipation - due to
   a. Subthreshold conduction through OFF Trs.
   b. Tunneling current through gate oxide
   c. Leakage through R.B diodes.

2. Dynamic Power dissipation - due to
   a. Charging & discharging of load capacitances
   b. "short-ckt" current while both pMOS & nMOS N/ws are partially ON.

$$P_{total} = P_{static} + P_{dynamic}$$

- Instantaneous power $P(t)$ drawn from the power supply is $\propto$ to supply current $i_{DD}(t)$ & the supply vtg V_{DD}.

$$P(t) = i_{DD}(t) V_{DD}$$

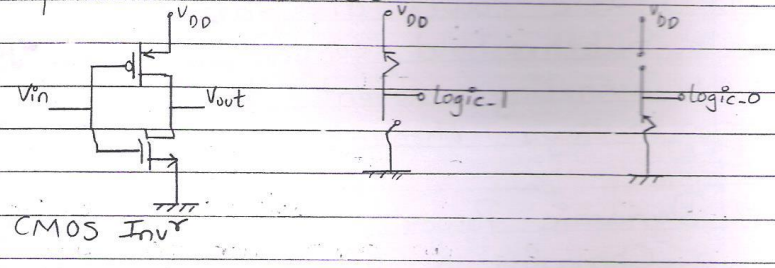
$$E = \int_0^T i_{DD}(t) V_{DD} \, dt$$

The average power over this interval is

$$P_{avg} = \frac{E}{T} = \frac{1}{T} \int_0^T i_{DD}(t) V_{DD} \, dt$$

Static Power Dissipation :-

Static CMOS gates are very power-efficient because they dissipate nearly zero power while idle.



CMOS Invr

Consider the static CMOS Invr, if I/p is 0/1, one of Tr is OFF ie $i(t)=0$

Hence, $P_{static} = 0W$; ideally

Zero static p.d is a principle adv of CMOS over other technology. However, secondary effects including sub-threshold conduction, tunneling and leakage lead to small amount of static current flowing through OFF Tr.

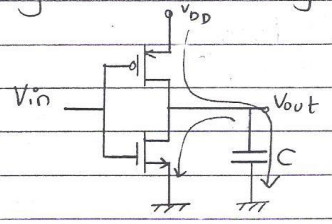
Assuming the leakage current is constant, the static p.d is the product of total leakage current & the supply voltage

$$P_{static} = I_{static} \cdot V_{DD}$$

- OFF Trs still conduct a small amt of subthreshold current which ↑ses as threshold vtgs are scaled down

Dynamic Power dissipation:-

- Primary component of dynamic p.d is charging & discharging of load capacitance.



- If a load C is switched between GND and V_{DD} at an avg freqⁿ of fsw i.e the load will be charged & discharged $T f_{sw}$ times. The current flows from V_{DD} to the load to charge it and it flows from load to gnd during discharge.
- In one complete charge/discharge cycle, a total charge of $Q = CV_{DD}$ is thus transferred from V_{DD} to GND.

The avg dynamic p.d is

$$P_{dynamic} = \frac{1}{T}\int_0^T i_{DD}(t)\,V_{DD}\,dt = \frac{V_{DD}}{T}\int_0^T i_{DD}(t)\,dt$$

$$P_{dynamic} = \frac{V_{DD}}{T}\left[T f_{sw} C V_{DD}\right]$$

$$\boxed{P_{dynamic} = C V_{DD}^2 f_{sw}}$$

f_{sw} - switching freqⁿ

∵ most of gates do not switch every clk cycle, it is more convenient to express f_{sw} as an activity factor α times the clk freqⁿ

∴ $\boxed{P_{dynamic} = \alpha C V_{DD}^2 f}$

$\alpha \rightarrow 0.1$ to 0.5

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• Summarise the approach you would take to reduce the p.d of a CMOS chip that is designed for palm top computer

• Low-Power Design :-

- Power dissipation has become extremely important to VLSI designers. For low power battery-based systems such as laptops, cell phones, power consumption sets the battery life of the product.
- Power reduction techniques can be divided into those that reduce dynamic power & those that reduce static power.

• Dynamic Power Reduction:-

$$P_{dynamic} = \alpha C V_{DD}^2 f \quad \text{watts}$$

Note:
$P_{dyn} \propto f$

The dynamic power is reduced by ↓sing α, the switching capacitance (C), power supply or the operating frequency.

a. Activity factor reduction:-
- Clocked nodes such as clk N/w have high activity factor of 1 and very power-hungry. Thus, dynamic ckt have high α, so they are costly in power.
- Clock gating can be used to stop portions of the chip that are idle.

Eg:
A floating point can be turned off when executing integer code.

- A large fraction of power is dissipated by the clk N/w itself, so entire portion of the clk N/w can be turned off where possible.
- A drawback of reducing α is that if the system transitions rapidly from an idle mode to fully active mode, a large di/dt spike will occur which will lead to inductive noise in power supply N/w. (power supply bounce).

b. Device switching capacitance (C) is reduced by choosing small Trs. It is most effectively reduced through careful floorplanning, placing communicating units near each other to reduce wire lengths.

c. Voltage reduction:-
Voltage has a quadratic effect on dynamic power. thus, choosing a lower power supply significantly reduces power consumption.
- If the frequency and vtg are scaled down in proportion, a cubic reduction in power is achieved.

d. Frequency can be traded for power. For eg. two multipliers running at half speed can replace a single multiplier at full speed. If power supply can be reduced because freqn requirement is lowered, overall power consumption goes down

• Static Power Reduction:-

Static power reduction involves minimizing I_{static}.

Subthreshold leakage current (I_{DS}) is

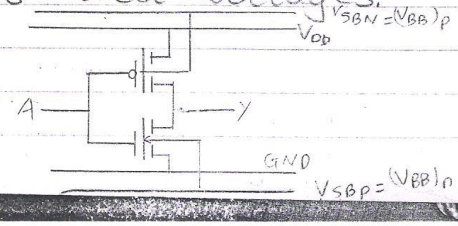
$$I_{DS} = I_{ds0}\, e^{\frac{V_{gs}-V_t}{nV_T}} \left[1 - e^{\frac{-V_{ds}}{V_T}}\right]$$

$$V_t = V_{to} - \eta V_{ds} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$$

where, 'γ' term describes body effect
'η' term describes DIBL.

- I_{DS} can be reduced by ↑sing V_{to}, reducing V_{gs}, V_{ds}, temperature & ↑sing V_{sb}.

- Leakage Current :-
Leakage current can be controlled through body voltage using body effect.
For example :-
Low-V_t devices can be used & reverse body bias (RBB) can be applied during idle mode, while higher-V_t devices can be used & then a forward body bias (FBB) can be applied during active mode.
Applying a body bias requires addnal power supply rails to distribute the substrate and well voltages.



- Source voltage can be raised in sleep mode which ultimately reduces V_{ds} and also gate leakage.
- Reducing V_{DD} in stand by mode reduces the DIBL contribution to leakage.
- Another mtd of reducing idle leakage current in low-power systems is to turn off the power supply entirely.
- Si on Insulator (SOI) ckts are attractive for low-leakage designs because they have a sharper threshold current rolloff.

- In a process with $K_p' = 75\mu A/V^2$, $V_{TP} = -0.4V$, $V_{DD} = 1.8V$. Calculate the static power dissp^n of a 32 word x 48 bit ROM that contains nMOS row decoder & pMOS pull-up in the 48 bit lines. The (W/L) ratio of pMOS pull-up is 1. Assume that 1 of the word line and 50% of bit lines are high at any given time

Soln:

$V_{GS} = V_{DD} = 1.8V$

For PMOS pull-up Tr,

$$I_{pull-up} = \frac{K_p'}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{TP})^2$$

$$= \frac{75\mu A}{2}(1)(1.8 - (-0.4))^2$$

$$= 181.5\ \mu A$$

Each PMOS Tr will dissipate power

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when o/p line is low

∴ Power dissipatn in 1 pull-up Tr is

$$P_{pull\text{-}up} = I_{pullup} \times V_{DD}$$
$$= 326.7\,\mu W$$

The total static p.d $= (326.7\mu W)\left(\frac{48}{2}+31\right)$

$$P_{static\ total} = 17.96\ mW.$$