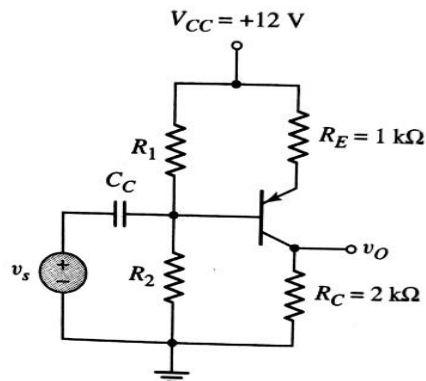
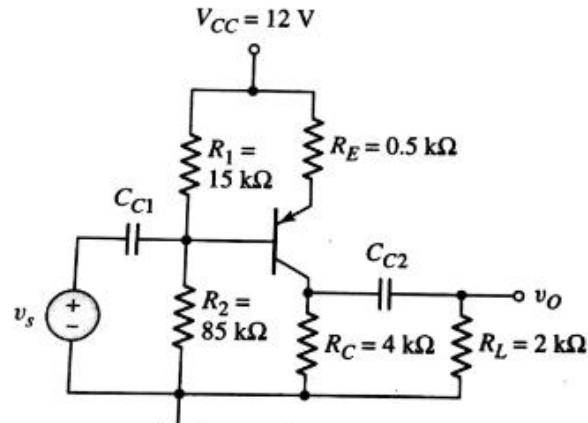
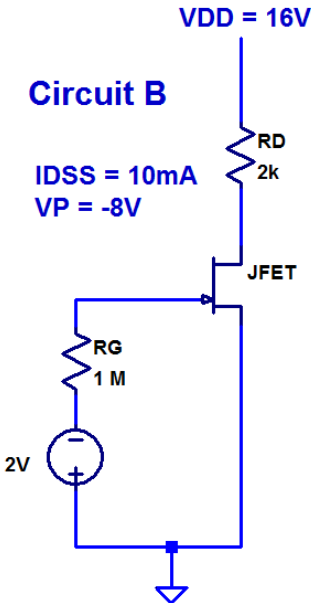


**K. J. Somaiya College of Engineering, Mumbai-77**  
 (Autonomous College Affiliated to University of Mumbai)  
 Semester: July – November 2019

**Max. Marks: 30**  
**Class: SY B. Tech**  
**Branch: ETRX**  
**Full name of the course : Basic Electronic Circuits**

**Duration: 1hr.15 min.**  
**Semester: III**  
**Re Test 2**  
**Course Code: 2UEXC302**

Q. No	Questions	Marks
Q.1	<p>The transistor parameters for the circuit in figure 1 are <math>\beta = 100</math> and <math>V_A = \infty</math>.</p> <p>a) Design the circuit such that it is bias stable and the Q point is in the center of load line.</p> <p>b) Determine small signal voltage gain of designed circuit.</p> <div style="text-align: center;">  <p><b>Figure 1</b></p> </div> <p style="text-align: center;"><b>OR</b></p> <p>The transistor in the circuit shown in figure 2 has parameters <math>\beta = 100</math>, <math>V_{EB(ON)} = 0.7V</math> and <math>V_A = \infty</math>.</p> <p>a) Determine quiescent collector current and emitter – collector voltage.</p> <p>b) Find small signal voltage gain</p> <div style="text-align: center;">  <p><b>Figure 2</b></p> </div>	15

<p>Q.2.</p>	<p>a) Draw circuit of Common source JFET amplifier. Hence, derive the expression of its voltage gain.</p> <p>b) N-channel JFET is rarely operated with positive value of gate to source voltage. Justify</p>	<p>5</p> <p>2</p>
<p>Q3.</p>	<p>Find <math>I_D</math>, <math>V_{GS}</math> and <math>V_{DS}</math> for circuit B</p>  <p><b>Circuit B</b></p> <p><math>V_{DD} = 16V</math></p> <p><math>R_D = 2k</math></p> <p><math>I_{DSS} = 10mA</math></p> <p><math>V_P = -8V</math></p> <p>JFET</p> <p><math>R_G = 1M</math></p> <p>2V</p>	<p>8</p>