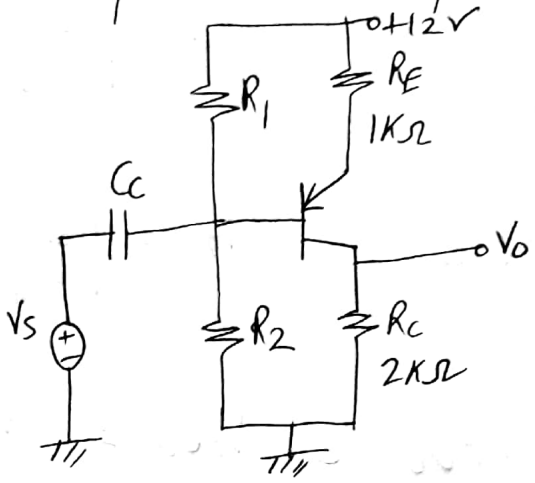
Re-test 2 Solution

Q1. pnp transistor parameters:- $\beta = 100$, $V_A = \infty$

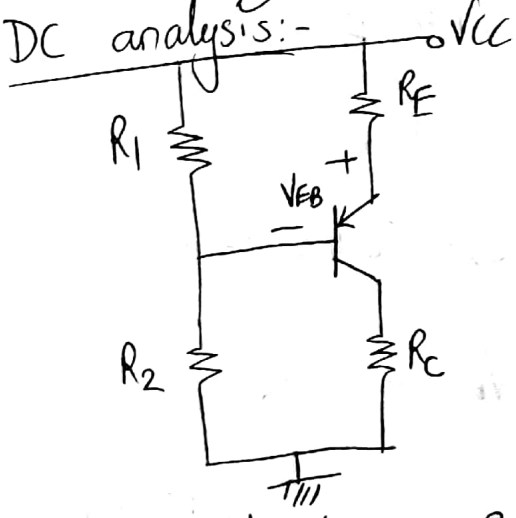


a) Design bias stable ckt such that Qpt is at center of load line

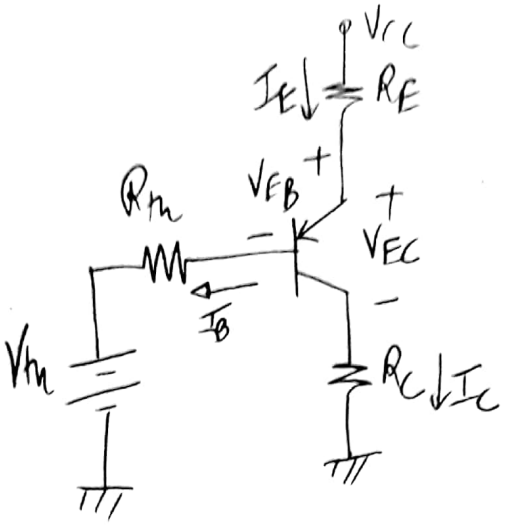
b) Determine small-signal voltage gain of designed ckt.

Soln:- A] 1) Above circuit is voltage-divider bias CE ckt with pnp transistor.

2) DC analysis:-



Applying thevenin's theorem & drawing equivalent ckt at base,



$$V_{th} = \frac{R_2}{R_1+R_2} V_{CC} \Rightarrow$$

$$R_{th} = \frac{R_2 R_1}{R_1+R_2} \Rightarrow$$

Given Q-pt is at center ie $V_{ECQ} = \frac{1}{2} V_{CC} = \underline{\underline{6V}}$

KVL to B-E loop gives,

$$V_{th} + I_B R_{th} + V_{EB} + I_E R_E - V_{CC} = 0$$

$$V_{th} + I_B R_{th} + V_{EB} + (1+\beta) I_B R_E - V_{CC} = 0$$

$$I_{BQ} = \frac{V_{CC} - V_{th} - V_{EB(on)}}{R_{th} + (1+\beta) \cdot R_E}$$

cannot do it since R_1 & R_2 is unknown!

KVL to B-C loop gives

$$V_{CC} - I_E R_E - V_{ECQ} - I_C R_C = 0$$

$$V_{CC} - \left(\frac{1+\beta}{\beta}\right) R_E I_{CQ} - V_{ECQ} - I_{CQ} R_C = 0$$

$$I_E = \left(\frac{1+\beta}{\beta}\right) I_C$$

$$I_{CQ} = \frac{V_{CC} - V_{ECQ}}{\left(\frac{1+\beta}{\beta}\right) R_E + R_C} = \frac{12-6}{\frac{101}{100} \times 1K + 2K_\Omega} \Rightarrow$$

$$\boxed{I_{CQ} = 1.99\ mA}$$

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1.99mA}{100} = 19.93\mu A \quad ; I_{EQ} = 2mA$$

→ For bias-stable ckt,

$$R_{th} = 0.1 \times (1+\beta) R_E = 0.1 \times 101 \times 1K\Omega = 10.1K\Omega$$

(10%)

→ $$V_{th} = \frac{R_2}{R_1+R_2} V_{CC} = \frac{R_{th}}{R_1} V_{CC} = \frac{10.1K}{R_1} \times 12 \quad -(1)$$

KVL to B-E loop gives,

$$V_{th} + I_{BQ}R_{th} + V_{EB(on)} + I_{EQ}R_E - V_{CC} = 0$$

$$V_{CC} = \underbrace{\frac{121.2K}{R_1}}_{V_{th}} + I_{BQ}R_{th} + V_{EB(on)} + 2mA \times R_E$$

$$12 = \frac{121.2K}{R_1} + 19.93\mu A \times 10.1K\Omega + 0.7 + 2mA \times 1K\Omega$$

$$R_1 \doteq 13.3K\Omega$$

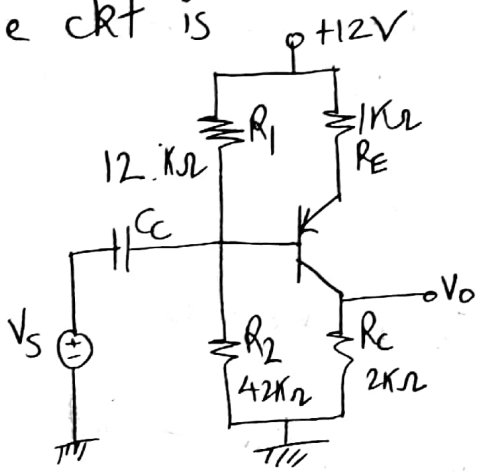
Select $\boxed{R_1 = 12\ K\Omega\ (std),\ 1/4W}$ L.S.V

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2} = 10.1K\Omega$$

$$10.1K\Omega = \frac{13.3K \times R_2}{R_2 + 13.3K} \Rightarrow R_2 = \underline{41.98K\Omega}$$

Select $\boxed{R_2 = 42K\Omega_{(std)},\ 1/4\,W}$

Bias-stable ckt is



B] $r_{\pi} = \frac{\beta V_T}{I_{CQ}} = \frac{V_T}{I_{BQ}} = \frac{26mV}{19.93\mu A} = \underline{1.3K\Omega}$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1.99mA}{26mV} = \underline{76.54\ \frac{mA}{V}}$$

$$A_V \simeq -\frac{R_C}{\frac{1}{g_m} + R_E} \approx -\frac{2K\Omega}{\frac{1}{76.54m} + 1K\Omega}$$ --- Degenerated CE stage

$$A_V \approx \frac{-2K\Omega}{13.065 + 1K\Omega} \approx \underline{-1.97}$$ --- small-sig voltage gain

OR

Q1 Given: pnp transistor parameters $\beta = 100$, $V_{EB(ON)} = 0.7V$, $V_A = \infty$

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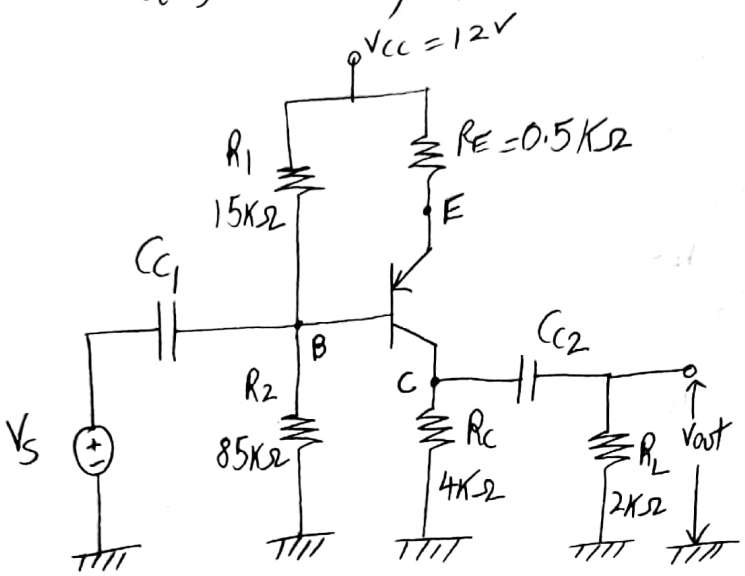
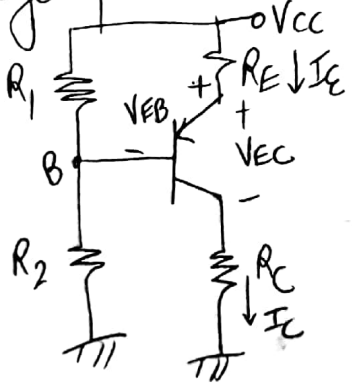


To find a) I_{CQ}, V_{ECQ}

b) Small-signal voltage gain

Soln: 1] DC Analysis :-

Notes- DC circuit of pnp transistor is same as that of npn device, expect that all current directions and voltage polarities are reversed.

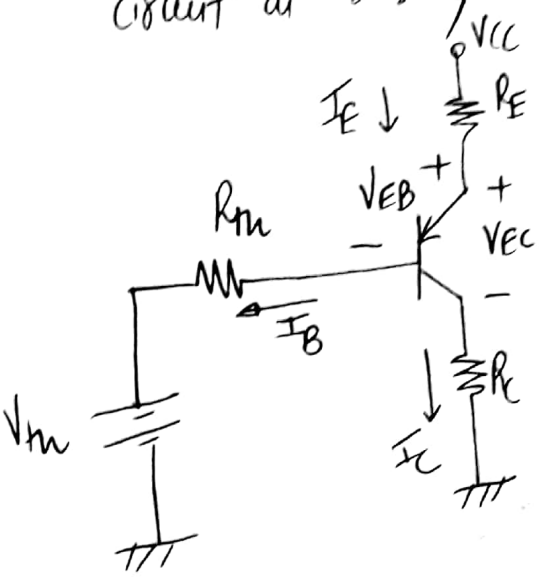


$R_{th} = R_1 \| R_2 = 15K \| 85K$

$R_{th} = \underline{12.75}\ K\Omega$

$V_{th} = \frac{R_2}{R_1+R_2} V_{CC} = \frac{85K \times 12}{85K+15K} = \underline{10.2V}$

Applying thevenin's theorem and drawing equivalent circuit at base, we get



KVL to B-E loop gives,

$$V_{Th} + I_B R_{Th} - V_{EB} + I_E R_E - V_{CC} = 0$$

$$V_{Th} + I_B R_{Th} - V_{EB} + (1+\beta) I_B R_E - V_{CC} = 0$$

$$I_{BQ} = \frac{V_{CC} - V_{Th} - V_{EB}}{R_{Th} + (1+\beta) R_E}$$

$$= \frac{12 - 10.2 - 0.7}{12.75 + 101 \times 0.5K}$$

$$I_{BQ} = 17.39 \mu A$$

ie $I_{CQ} = \beta I_{BQ} = 100 \times 17.39 \mu A$

$$\boxed{I_{CQ} = 1.74 \text{ mA}}$$

KVL to C-E loop gives,

$$V_{CC} - I_E R_E - V_{EC} - I_C R_C = 0$$

$$I_E = I_B + I_C = 1.757\,mA$$

$$V_{EC} = V_{CC} - I_E R_E - I_C R_C$$

$$= 12 - 1.757mA \times 0.5K - 1.74mA \times 4K\Omega$$

$$\boxed{V_{EC} = 4.16\,V}$$

2] Small-signal parameters:-

Note:- For pnp bjt, all small-sig parameters (g_m, r_π, r_o) formula remains same.

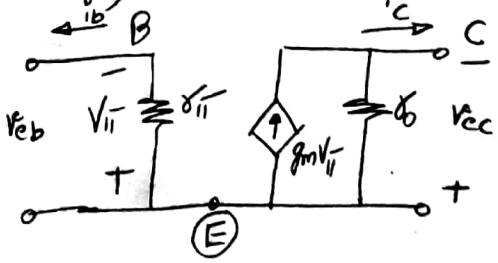
a) $r_\pi = \frac{V_T}{I_{BQ}} = \frac{26mV}{17.39\mu A} = 1.495K\Omega$

b) $g_m = \frac{I_{CQ}}{V_T} = \frac{1.74mA}{26mV} = 66.92\frac{mA}{V}$

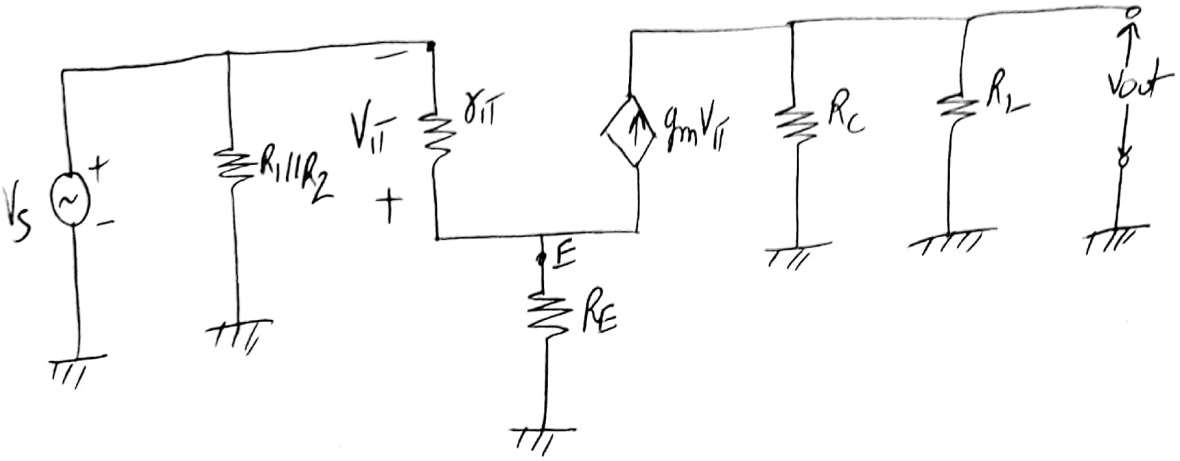
c) $r_o = \frac{V_A}{I_{CQ}} = \infty$

3] Small-sig hybrid-π model (pnp transistor)

Hybrid-π model of pnp bjt is same as that of npn bjt; except that all current directions & voltage polarities are reversed.



Small-sig equivalent circuit:-



- The above equivalent ckt is similar to CE degenerated stage with npn transistor,

$$A_v \simeq -\frac{(R_C \| R_L)}{\frac{1}{g_m} + R_E}$$

$$A_v \approx -\frac{(2K\Omega \| 4K\Omega)}{\frac{1}{66.92\frac{mA}{V}} + 0.5K\Omega}$$

$$\approx -\frac{1.33K\Omega}{14.94 + 0.5K}$$

$$\boxed{A_v \approx -2.58}$$

→ Small-signal voltage gain

Retest 2 - BEC

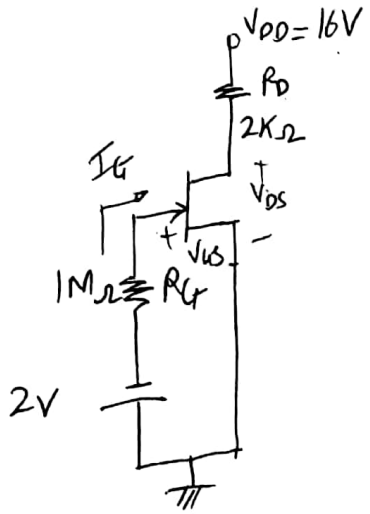
Q2 a) Circuit of Common source JFET amplifier ------- 1M

Small-signal equivalent ckt ------- 1M

Derivation for voltage gain ------- 3M

Q2 b) Justification:
N-channel JFET is rarely operated with positive value of gate to source voltage ------- 2M

Q3)



$I_{DSS} = 10mA$
$V_P = -8V$

Soln → KVL to G-S loop,

$-2 - I_G R_G - V_{GS} = 0$

$I_G = 0$ for JFET

$V_{GSQ} = -2V$ ----- 2M

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10mA\left(1 - \frac{(-2)}{(-8)}\right)^2 = 5.625\,mA$ --- 3M

KVL to D-S loop, $V_{DD} - I_D R_D - V_{DS} = 0 \Rightarrow V_{DS} = V_{DD} - I_D R_D$

$V_{DS} = 4.75V$ -- 3M