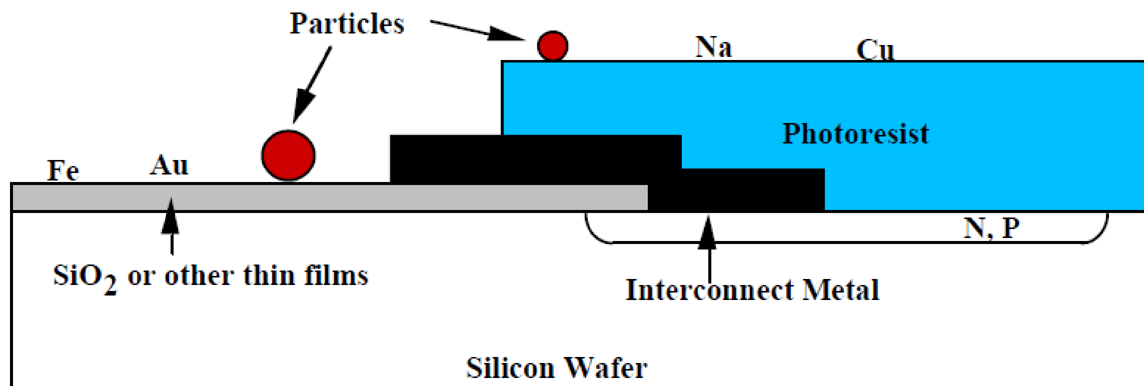
Wafer Cleaning

- Surface films and doped regions must not be significantly attacked.
- Photoresist strip and particle removal typical
- Room air and process equipment delivered particles
  - Significant elements that cause severe problems in silicon include: organics, metals (Fe, Au, Cu, etc.) and alkali ions (Na, K, etc.)



Example Sensitivity

- Example #1: MOS transistor gate threshold shift

MOS V_{TH} is given by $$V_{TH} = V_{FB} + 2\phi_f + \frac{\sqrt{2\varepsilon_S q N_A (2\phi_f)}}{C_O} + \frac{qQ_M}{C_O} \quad (1)$$

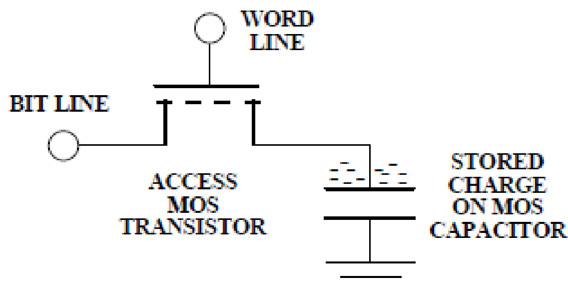
  – Q_M is the mobile charge density (number of charges per cm^2) of Na^+ and K^+ in the gate oxide

If t_{ox} = 10 nm, then a 0.1 volt V_{th} shift can be caused by $Q_M = 6.5 \times 10^{11}$ cm^{-2} (< 0.1% monolayer or 10 ppm in the oxide).

  – Prevented MOS technologies initially from being important commercially!

Example Sensitivity

- Example #2: MOS DRAM
  – Storage of charge based on minimal charge leakage in time.
    - Refresh required to maintain charges after a technology defined period of time.
  – Dominated by Shockley, Reed Hall (SRH) recombination (intermediate impurity related energy levels).
    - σ is the trap cross sectional area, ($10^{-15}cm^{-2}$) v_{th} is the minority carrier thermal velocity (10^7 cm/sec), and N_t is the density of traps.
    - Deep-level traps (Cu, Fe, Au etc.) Pile up at the surface where the devices are located.



- **Refresh time of several msec requires a generation lifetime of**

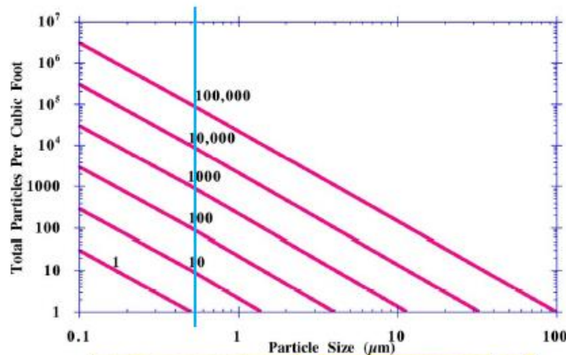
$$\tau_R = \frac{1}{\sigma \cdot v_{th} \cdot N_t} \approx 100\ \mu\text{sec} \quad (2)$$

- **This requires $N_t \approx 10^{12}$ cm^{-3} or ≈ 0.02 ppb (see text).**

Clean Factories – Wafer Fab Facility

- The wafer fabrication area "Clean Rooms" must particle free.
  - Sources of particles
    - Air (normal presence of particles) and Water
    - Machinery – particularly due to friction, metals
    - People – 5 to 10 million particles per minute, organic
    - Supplies – brought in to room for use
    - Processing
  - Rooms and People
    - Clean room limited access, finger wall machine access
    - Bunny suits, gloves, air showers, covered faces/facemask
    - Glove box and robots
  - Air handling
    - Positive air pressure, HEPA filters

Level 1 Contamination Reduction: Clean Factories



- Air quality is measured by the "class" of the facility.
  - Less than X total particles greater than 0.5 um per cubic foot of air.

(Photo courtesy of Stanford Nanofabrication Facility.)

Factory environment is cleaned by:

- HEPA filters (99.07% eff.)
- Air recirculation (laminar >50 cm/sec)
- Bunny suits for workers
- Filtration of chemicals and gases
- Manufacturing protocols

Wafer Cleaning

- Remove particles, films such as photoresist, and any other trace contaminants
- Distinct processes
  - Silicon wafer clean (frontend processes)
  - Post metalization clean (backend processes)
- Frontend Wafer Cleaning based on RCA process
  - RCA was originally the Radio Corporation of America
  - Werner Kern developed the basic procedure in 1965 while working for RCA.
- The RCA clean involves the following :
  1. Removal of the organic contaminants (Organic Clean)
  2. Removal of thin oxide layer (Oxide Strip)
  3. Removal of ionic contamination (Ionic Clean)

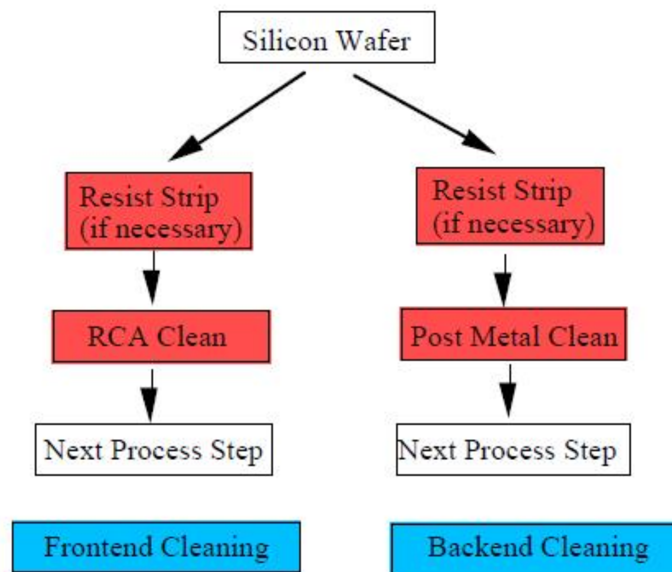
Frequently used Chemicals

Chemical Name	Purpose
Acetone	Wafer Cleaning and Resist removal
Iso Propyl Alcohol	Wafer Cleaning
Methanol	Cleaning
Trichloro Ethylene	III-V wafer cleaning
Acetic Acid	Constituent of HNA for Si/Poly Si etching
Hydrofluoric Acid	Silicon Dioxide, Silicon Nitride etching
Hydrochloric Acid	RCA Cleaning
Phosphoric Acid	Silicon Nitride Etching
Sulphuric Acid	Piranha
Nitric Acid	Constituent of HNA for Si/Poly Si etching
Ammonium Hydroxide	RCA Cleaning
Tetra methyl Ammonium Hydroxide	Anisotropic etching of Si

The RCA Clean

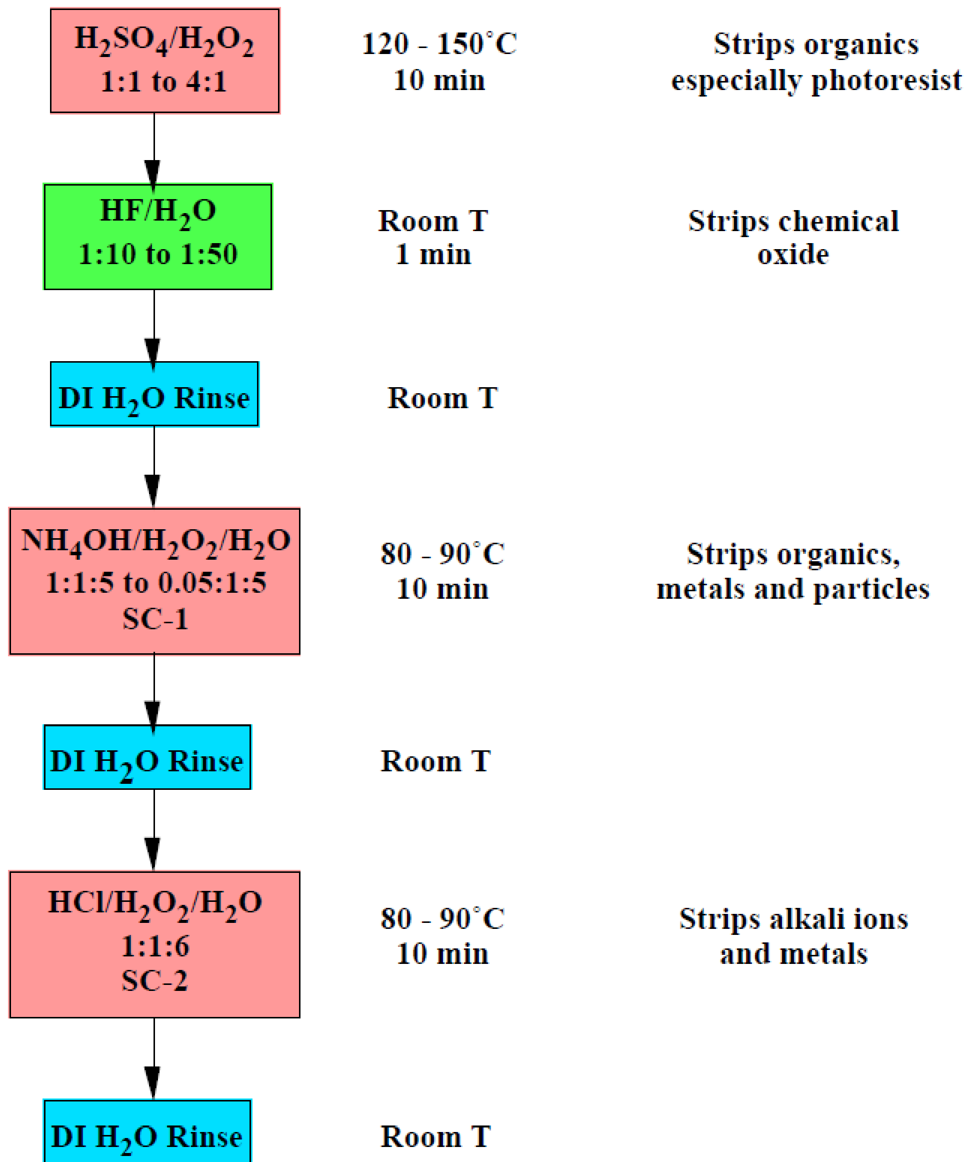
- The first step (called SC-1, where SC stands for Standard Clean) is performed with a 1:1:5 solution of NH_4OH + H_2O2 + H_2O at 70º to 80º C for 10 minutes.
  - This treatment oxidizes organic films and complexes Group IB and IIB metals as well as Au, Ag, Cu, Ni, Zn, Cd, Co, and Cr. The solution dissolves and regrows a thin native oxide layer on the silicon.
- The next step is a short immersion in a 1:50 solution of HF + H2O at 25º C
  - Remove the thin oxide layer and some fraction of ionic contaminants.
- Perform a DI rinse.
- The next step (called SC-2) is performed with a 1:1:6 solution of HCl + H_2O_2 + H_2O at 70º to 80º C for 10 minutes.
  - This treatment removes alkali ions and cations (AL, Fe, Mg) that form NH_4OH insoluble hydroxides in solutions like SC-1. In SC-2 they for soluble complexes. This solution also completes the removal of metal contaminants.
- Perform a DI rinse

Level 2 Contamination Reduction: Wafer Cleaning



(Photo courtesy of Ruth Carranza.)

- **RCA clean is "standard process" used to remove organics, heavy metals and alkali ions.**


H_2SO_4/H_2O_2
1:1 to 4:1
120 - 150°C
10 min
Strips organics
especially photoresist
HF/H_2O
1:10 to 1:50
Room T
1 min
Strips chemical
oxide
DI H_2O Rinse
Room T
$NH_4OH/H_2O_2/H_2O$
1:1:5 to 0.05:1:5
SC-1
80 - 90°C
10 min
Strips organics,
metals and particles
DI H_2O Rinse
Room T
$HCl/H_2O_2/H_2O$
1:1:6
SC-2
80 - 90°C
10 min
Strips alkali ions
and metals
DI H_2O Rinse
Room T

De-Ionized (DI) Water

- Clean water for silicon processing
- DI Water conductivity example:

DI water is necessary: $H_2O \leftrightarrow H^+ + OH^-$ with $[H^+]=[OH^-]=6x10^{-13}cm^{-3}$
Diffusivity of : $H^+ \approx 9.3x10^{-5}cm^2s^{-1}$ $\rightarrow \mu_{H+}=qD/kT=3.59cm^2V^{-1}s^{-1}$
of : $OH^- \approx 5.3x10^{-5}cm^2s^{-1}$ $\rightarrow \mu_{OH-}=qD/kT=2.04cm^2V^{-1}s^{-1}$

$$\rho = \frac{1}{q([H^+]\mu_{H^+} + [OH^-]\mu_{OH^-})} = 18.5 M\Omega cm$$

Distilled water is typically 10 uS/cm or 0.1 MΩ cm

Gettering

- Removing trace elements from active transistor locations by causing them to combine with defects in the silicon.
  - Active devices cover a very small portion of the silicon volume, typically near one surface.
  - Metals and alkali ions have very high diffusivity.
  - They tend to be easily captured either in regions with mechanical defects or in regions which chemically trap them.
- For the alkali ions, gettering generally uses dielectric layers on the topside (PSG or barrier Si3N4 layers).
- For metal ions, gettering generally uses traps on the wafer backside (extrinsic) or in the wafer bulk (intrinsic).

Level 3 Contamination Reduction: Gettering

- Gettering is used to remove metal ions and alkali ions from device active regions.

Alkali Ions

Deep Level Impurites in Silicon

Period	I	II	III	IV	V	VI	VII	VIII	VIII	VIII	I	II	III	IV	V	VI	VII	Noble Gases
1	1 H 1.008																	2 He 4.003
2	3 Li 6.941	4 Be 9.012											5 B 10.81	6 C 12.01	7 N 14.01	8 O 16.00	9 F 19.00	10 Ne 20.18
3	11 Na 22.99	12 Mg 24.31											13 Al 26.98	14 Si 28.09	15 P 30.97	16 S 32.06	17 Cl 35.45	18 Ar 39.95
4	19 K 39.10	20 Ca 40.08	21 Sc 44.96	22 Ti 47.88	23 V 50.94	24 Cr 51.99	25 Mn 54.94	26 Fe 55.85	27 Co 58.93	28 Ni 58.69	29 Cu 63.55	30 Zn 65.39	31 Ga 69.72	32 Ge 72.59	33 As 74.92	34 Se 78.96	35 Br 79.90	36 Kr 83.80
5	37 Rb 85.47	38 Sr 87.62	39 Y 88.91	40 Zr 91.22	41 Nb 92.91	42 Mo 95.94	43 Tc 98	44 Ru 101.1	45 Rh 102.9	46 Pd 106.4	47 Ag 107.9	48 Cd 112.4	49 In 114.8	50 Sn 118.7	51 Sb 121.8	52 Te 127.6	53 I 126.9	54 Xe 131.3
6	55 Cs 132.9	56 Ba 137.3	57 La 138.9	72 Hf 178.5	73 Ta 180.8	74 W 183.9	75 Re 186.2	76 Os 190.2	77 Ir 192.2	78 Pt 195.1	79 Au 197.0	80 Hg 200.6	81 Tl 204.4	82 Pb 207.2	83 Bi 209.0	84 Po 209	85 At 210	86 Rn 222
7	87 Fr 223	88 Ra 226	89 Ac 227.0	104 Unq 261	105 Unp 262	106 Unh 263	107 Uns 262											

Shallow Acceptors

Elemental Semiconductors

Shallow Donors

- For the alkali ions, gettering generally uses dielectric layers on the topside (PSG or barrier Si_3N_4 layers).

- For metal ions, gettering generally uses traps on the wafer backside or in the wafer bulk.

- Backside = extrinsic gettering.

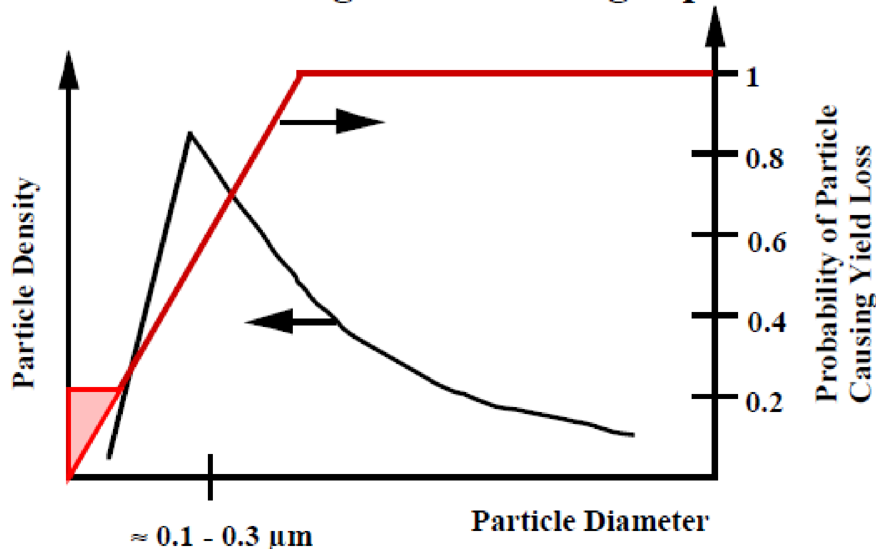
- Bulk = intrinsic gettering.

<u>**Modeling Particle Contamination and Yield**</u>

- ≈ 75% of yield loss in modern VLSI fabs is due to particle contamination.

- Yield models depend on information about the distribution of particles.

- Particles on the order of 0.1 - 0.3 μm are the most troublesome:
  - larger particles precipitate easily
  - smaller ones coagulate into larger particles



- Yields are described by Poisson statistics in the simplest case.

$$Y = \exp^{-A_C D_O} \qquad (3)$$

where A_C is the critical area and D_O the defect density.

- This model assumes independent randomly distributed defects and often underpredicts yields.

Summary of Key Ideas

- A three-tiered approach is used to minimize contamination in wafer processing.
- Particle control, wafer cleaning and gettering are some of the "nuts and bolts" of chip manufacturing.
- The economic success (i.e. chip yields) of companies manufacturing chips today depends on careful attention to these issues.
- Level 1 control - clean factories through air filtration and highly purified chemicals and gases.
- Level 2 control - wafer cleaning using basic chemistry to remove unwanted elements from wafer surfaces.
- Level 3 control - gettering to collect metal atoms in regions of the wafer far away from active devices.
- The bottom line is chip yield. Since "bad" die are manufactured alongside "good" die, increasing yield leads to better profitability in manufacturing chips.

Acknowledgements

1. J.D Plummer , Deal and Griffin, Silicon VLSI Technology Fundamentals, Practice and Modeling.
2. Centre of Excellence in Nanoelectronics, IITB
3. http://www.cen.iitb.ac.in/cen/safety/chemRoom.php