Module: 6.2

Nanowire:Fabrication and applications

Reference Book: James E. Morris "Nanoelectronic Device Applications Handbook", CRC Press

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What are nanowires?

Nanowires are **microscopic wires** that have a width measured in nanometers. Typically their width ranges from **forty to fifty nanometers**, but their length is not so limited. Since they can be lengthened by simply attaching more wires end to end or just by growing them longer, they can be as long as desired.

What Are Nanowires Made of?

Nanowires are **metal** just like other, regular wires. The only real difference in concept is their size. They also vary in complexity and uses. While they can do many of the same things, they have many other capabilities beyond those of regular wire.=

What good are nanowires?

Some uses of nanowires include:

• Data storage/transfer - transfer data up to **1,000 times faster**, and store data for as long as **100,000 years without degradation**

• Batteries/generators - tiny, efficient solar panels, turning light into energy, able to hold **10 times the charge** of existing batteries

• Transistors

• LED's

• Optoelectronic devices

• Biochemical sensors

• Heat-pumping Thermoelectric devices

Striped Nanowires?

Striped nanowires are capable of performing **more than one task** along the same wire. They are striped with **different materials** that posses different properties, an attribute which allows different operations to be performed at the same time. This also enables devices to be more compacted because fewer wires are needed; each nanowire is serving multiple functions.

What uses are nanowires being developed for?

IBM has been doing research on forming U-shaped nanowires to create a **"racetrack memory"**. This method would allow IBM to create a memory system with no moving parts and far **greater storage** than flash memory. This U-shape is formed with closely arranged nanowires, allowing fast transmissions and increasing storage size without adding to the overall size of the device.

Nanowires are also being developed for **prototype sensors**. These sensors will be used on gases and biological molecules. They will be used to detect harmful agents by scanning each gas or chemical on a molecular level. This is possible due to how small these wires can be. They will be

made out of materials that react to harmful agents, thus alerting to the presence of harmful agents. For Star Trek fans, this would be a very similar device to the "Tri- Corder."

Why Are Nanowires Not Being Implemented?

Nanowires are not being heavily manufactured because they are still in the **development stage** and are only produced in the laboratory. Until production has been streamlined,made easier and faster, they will not be heavily manufactured for commercial purposes. Furthermore, though they are **4 or 5 times more effective** than current technology, an industry-wide technology overhaul is **not cost effective** at the moment.

Introduction:

Due to the high surface to volume silicon ratio and unique quasi one dimensional electronic structure, silicon nanowire based devices have properties that can outperform their traditional counterparts in many ways. To fabricate silicon nanowires, in principle there are a variety of different approaches. These can be classified into top-down and bottom-up methods. The choice of fabrication method is strongly linked to the target application. From an application point of view, electron devices based on silicon nanowires are a natural extension of the downscaling of a silicon metal insulator semiconductor transistor. However, the unique properties also allow implementing new device concepts like the junctionless transistor and new functionalities like reconfigurability on the device level. Sensor devices may benefit from the high surface to volume ratio leading to a very high sensitivity of the device.
Also, solar cells and anodes in Li-ion batteries can be improved by exploiting the quasi one-dimensionality. This chapter will give a review on the state-of-the-art of silicon nanowire fabrication and their application in different types of devices.

Silicon nanowires are quasi one-dimensional (1D) structures with a diameter of less than 100 nm. The very small diameter results in a large surface to volume ratio. This can be exploited in many ways in electronic devices. When a gate is wrapped around the nanowire, the optimum control of the nanowire potential by the gate potential is ensured. This makes nanowires an excellent choice for the ultimate silicon metal insulator semiconductor (MIS) devices. However, the same feature also allows implementing device concepts that would have very poor properties in a conventional planar configuration. The junctionless transistor and tunnel field effect transistors are two prominent examples. Additionally, new types of functionalities can be exploited by making the devices reconfigurable. When it comes to sensing devices, the small volume will allow effectively controlling the potential of the nanowire by even a very small input signal, making the approach very sensitive specifically for chemical sensing and bio-sensing. But also the field of energy generation and storage can benefit from the quasi 1D structure. In the solar cells the nanowires allow to more efficiently collect the incoming solar radiation whereby in Li-ion batteries the structure allows for volume expansion.

A large number of techniques exist to fabricate silicon nanowires. These can beclassified into bottom-up and top-down fabrication techniques. In top-down fabrication,lithography is used to define the fabricated structure that is then transferredfrom the photo-resist to the substrate by etching or a similar way of structuring thealready available material. In the bottom-up approach, the material is added to thesubstrate in a self-organized way.

Fabrication Techniques for Silicon Nanowires

Traditionally semiconductor technology is driven by top-down fabrication using photo lithography. This approach has successfully enabled to scale down device dimensions all the way to the 10 nm range. In contrast, bottom-up techniques have the potential to construct very complex structures without the need of defining them in all details by a mask. Nevertheless, there are still some missing links to make the bottom-up approach a manufactural alternative. When it comes to silicon nanowires, both paths are possible and have their advantages and drawbacks. In the top-down fabrication, a clear path from today's planar and FinFET devices to nanowire devices can be drawn. However, the etching of the nanowire out of the bulk silicon results in non-perfect geometry and requires advanced lithography. The bottom-up approaches, on the other hand, may lead to excellent crystal quality and small diameter using a very simple process. The precise placement and generation of highly complex structures as integrated circuits still remains elusive. Therefore, also combinations of both paradigms are considered. Another alternative is to use a template made from an insulating material like silicon dioxide or aluminium oxide, etch holes into the layer and fill the holes with silicon or the desired semiconductor material. This can be considered as a top-down fabrication process for vertical nanowires. The traditional top-down process, in contrast, will result in horizontal nanowires although etching wires out of a bulk crystal is in principle also possible.

The vapour liquid solid(VLS) method for growing nanowires involve the chemical reaction between gaseous reactants and a liquid or molten catalyst to form nanowires on a solid substrate. VLS is the most attractive method for growing high purity, single crystal nanowires.
As shown in figure 1(a) there are three stages in the VLS growth mechanism:

1) Alloying
2) Nucleation and
3) Axial growth

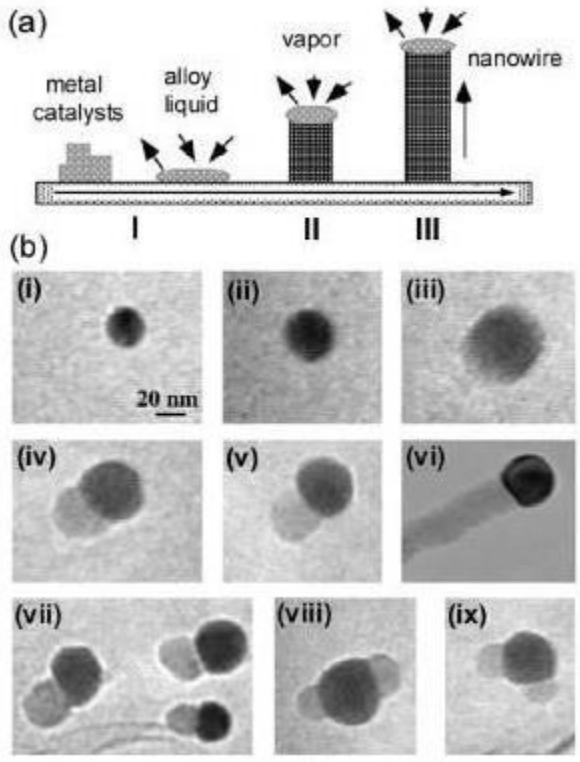


Figure 1(a) Schematic of VLS germanium nanowire growth mechanism including three stages (I) alloying, (II) nucleation, and (III) axial growth
(b) In situ TEM images recorded during the process of Ge nanowire growth

The nanowires produced generally have alloy droplets on their tips. The example shown in figure 1(b) typifies the process which includes a solid catalyst that forms an alloy with a gaseous reactant at elevated temperatures. The alloy then becomes supersaturated with the reactant, which causes nucleation of the nanowire and preferential axial precipitation (growth) of the nanowire from the liquid alloy surface. Using this process, single crystal nanowires composed of silicon, germanium, ZnO, GaN, and SnO2 have been fabricated. Core-shell nanowires can also be fabricated by this method. Other similar techniques, such as supercritical fluid-liquid-solid(SFLS) or supercritical fluid-solid-solid(SFSS), and solution-liquid-solid(SLS) methods have been used to fabricate Si, Germanium, and CdSe nanowires.
For top-down fabrication of nanowires well-established technologies from silicon VLSI circuit technology can be applied. To form horizontal nanowires that are electrically isolated from the substrate, two approaches are commonly used. In the simplest approach, a SOI substrate is used and the nanowire is etched into the thin active silicon layer using an anisotropic etching process. In the other approach bulk silicon and a deep reactive ion etch (DRIE) process are used together to structure a stack of nanowires. Figure 1.3 shows both approaches schematically. The latter approach has the beauty that the footprint is small and there will be several parallel nanowires to carry the current in a device using nanowires from such a procedure. Figure 1.4 shows examples of nanowires created by both techniques.

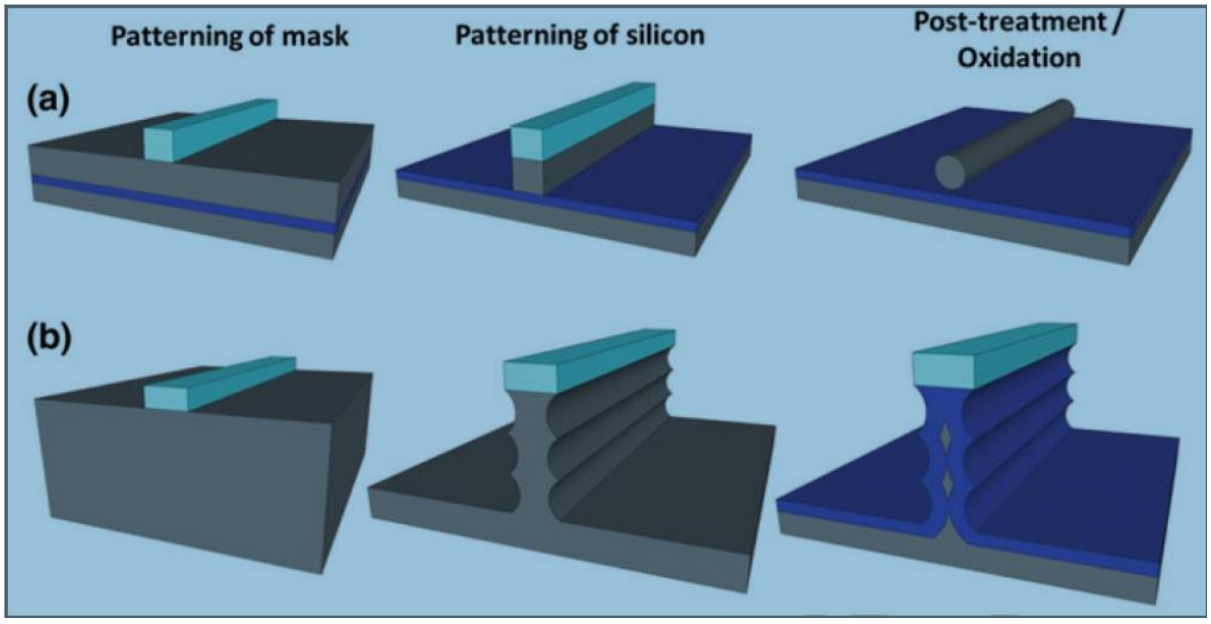


Fig. 1.3 Horizontal silicon nanowires fabricated by top down fabrication. a Starting with SOI substrate and etching using anisotropic reactive ion etching. b Starting with bulk substrate and etching with deep reactive ion etching and subsequent oxidation.

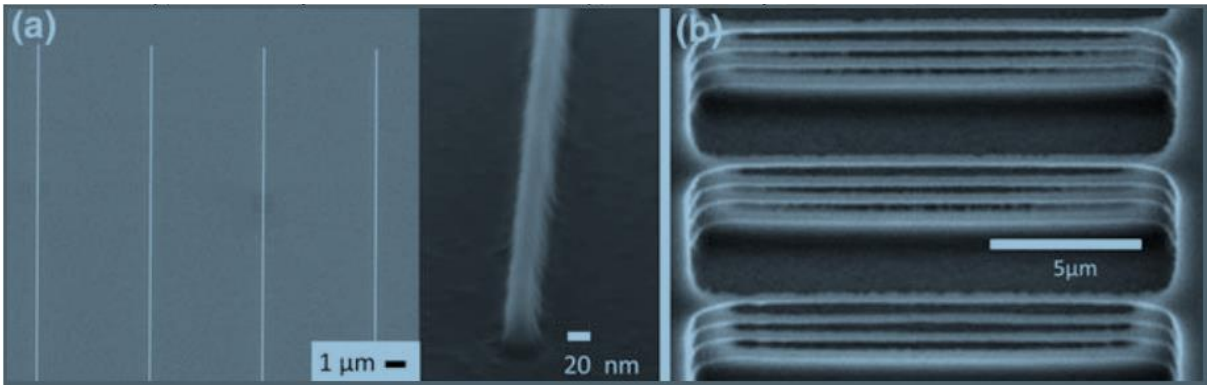


Fig. 1.4 Examples of horizontal silicon nanowires achieved by top-down fabrication. a Nanowires with 20 nm height and 25 nm widths produced using an SOI substrate. b Close up view of the nanowires form on the SOI substrate. b Nanowires formed using the deep reactive ion etch (DRIE) process © 2009 IEEE.

This process involves the formation of nanowires from a liquid precursor, usually in the presence of a catalyst or molecular template. One common example is the reduction of silver or gold salts in the presence of polymers or surfactants such as polyvinylpyrrolidone(PVP) or cetyltrimethylammonium bromide(CTAB). The surfactants adsorb preferentially on specific crystalline faces and enhance or inhibit growth along those faces, thereby resulting in the spontaneous growth of nanowires(along the planes in which growth is preferred). In certain cases, solid crystalline seeds are also added to the solution, to initiate preferential axial growth along specific crystal faces. As an example, gold nanorods were prepared by the addition of about 4nm gold nanospheres as seeds and the subsequent reduction of metal salt with a weak reducing agent in the presence of a surfactant to produce nanorods. By adding another component such as ascorbic acid, metal was preferentially deposited at the ends of the rods to form Dog-bone like nanowires. In solution, a variety of parameters such as temperature, concentrations and surfactants can be varied to gain some control over the type of nanowires formed.

Electrodeposition in nanoporous templates:
This method employs physical templates to direct the growth of nanowires within nanoporous membranes. Nanoporous membranes are fabricated using track etching or anodic electrochemical methods; these membranes are also commercially available with pore sizes ranging from 15nm to 500nm and membrane thickness up to 60 μm. Briefly the process Fig15 (a) involves sealing one face of the membrane with a conductive seed layer. This seed layer is usually deposited onto the membrane using thermal or sputter evaporation. Single segment or multisegmented nanowires are then deposited in the membrane using an electrolytic solution containing the appropriate ions. The seed layer and a counter electrode immersed in the solution form the electrolytic cell. The length of the segments within the nanowires is restricted by controlling the current density or voltage, and the duration of electrodeposition process. Electrodeposition in templates is the most attractive method to fabricate nanowires with multiple segments Fig 1.5b and theoretically can be used to fabricate nanowires composed of any material that can be electrodeposited.

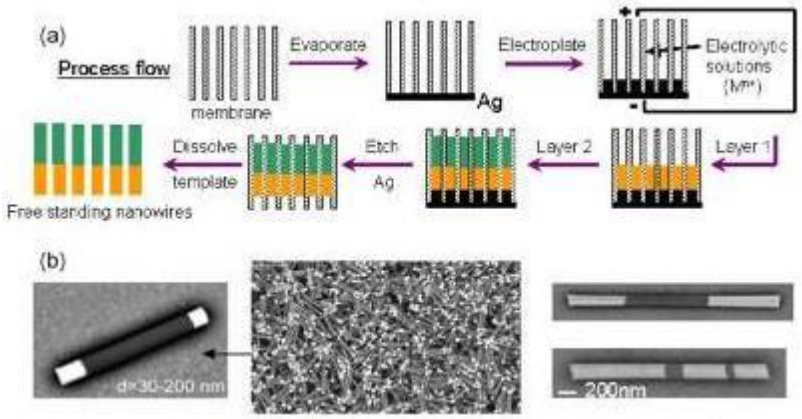
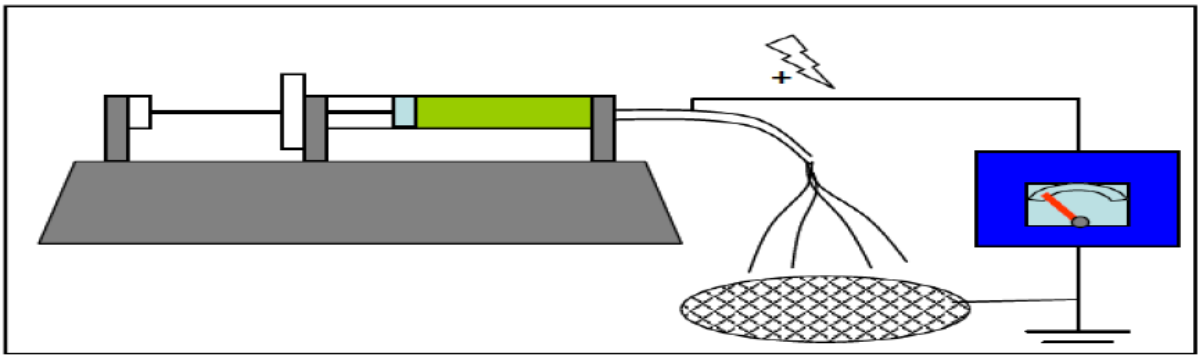


Figure 1.5 (a) Schematic of nanowire fabrication process using electrodeposition in nanoporus templates (b) several examples of fabricated multisegment nanowires.

Electrospinning:
Electrospinning is a simple and efficient way to produce polymeric nanowires, also called nanofibers. The basic set-up utilizes a syringe through which polymer solutions are driven; their

surface tension at the tip, under high electric field, can be overcome resulting in the ejection of a charged jet. The electrical forces elongate the jet thousands or even mollions of times and the jet becomes very thin, down to nanoscale. After the solvent evaporates, or melt solidifies, long polymeric nanofibers can be collected on an electrically grounded metal sheet. As compared to other fabrication methods, electrospinning facilitates the formation of extremely long nanowires with well controlled curvature.



(Basic setup of electrospinning technique)

Applications of Silicon nanowire:

Electron Devices Based on Silicon Nanowires Silicon exhibits unique properties when it acquires a 1D shape. Quantum confinement of electrons and holes is predicted to be substantial only at aggressive diameters below of 3 nm. Note that this is in contrast to III–V semiconductors, where confinement is visible already at larger diameters. Therefore, it makes sense to denote the behavior of Si nanowires as quasi 1D. The band structure is strongly modified for Si nanowires with diameters below of 10 nm. The band gap increases for smaller diameters and a direct band gap can be obtained for sufficiently small diameters. The quasi 1D behavior of silicon nanowires with very small dimensions can be utilized in devices in many different ways. For field effect devices, when the gate electrode is wrapped around the nanowire, the optimum geometric gate coupling can be provided to the active region. In addition to this, if the silicon thickness is small enough to allow a full depletion at low voltages the best scaling behavior of the device can be achieved. A useful parameter to characterize the gate control over the channel is the natural or screening length. It describes the efficiency of bending the energy bands and depends on the gate geometry, gate dielectric, nanowire thickness and doping concentration. Depending on the density of states nanowire field effect devices can be designed to operate either in a classical gate capacitance limited mode or the quantum capacitance limit. In the latter the channel charge remains constant when scaling down the gate oxide thickness leading to an improved power to delay product.

Using scaled nanowires, very promising circuit demonstrations have already been shown. Another more conventional approach comes from semiconductor memories, especially NAND Flash. For decades, the dilemma between fast erase and retention is hindering the full success of charge trapping devices. The underlying physical reason is that the field in the tunnel oxide and the top oxide cannot be controlled independently of each other like this can be done in a floating gate device. Generally speaking, it is necessary to enhance the field in the tunnel oxide and possibly at the same time reduce the field in the top oxide. Nanowires and to a lower extent tri-gates offer a unique opportunity here, since the geometry will automatically generate a higher field at the bottom oxide and the extension of the field increase can be controlled by the diameter of the nanowire. Figure 1.6 illustrates that situation. However, up to now the technological hurdle for introducing nanowires to push charge trapping applications is too high, as long as a cheaper scaling can be achieved using floating gates. Since almost ten years intense research has been started to explore the third dimension in NAND memory cell.

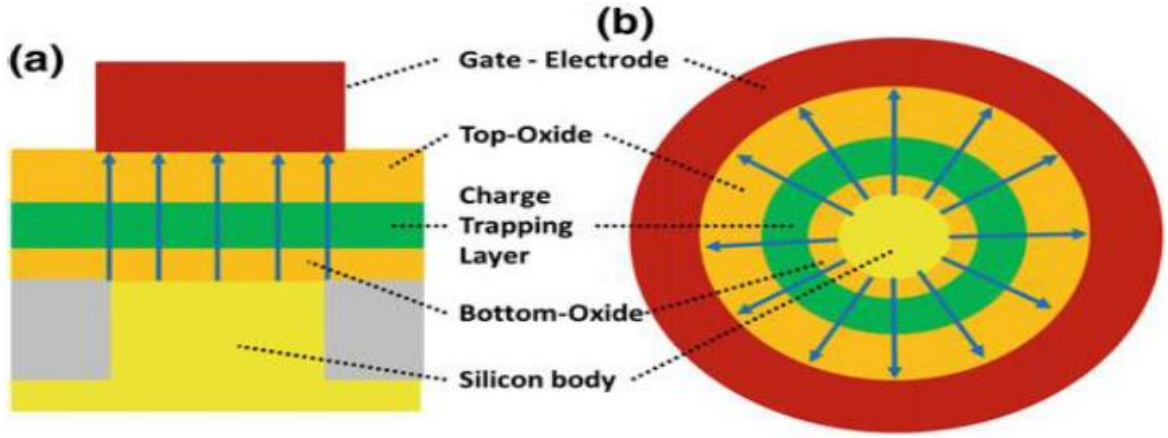


Fig. 1.6 Schematic cut in width direction of a planar (a) and a nanowire based (b) charge trapping

The arrows indicate the field lines in the device in programing or erase operation. In the nanowire device the field lines are denser in the bottom oxide. Therefore the exchange of carriers between the charge trapping layer and the silicon transistor body is enhanced and the charge exchange between the charge trapping layer and the gate-electrode is reduced flash memories, which might turn this cost per function relation. It was shown that by using concepts where many layers can be fabricated and then connected by a single or a few lithography steps is necessary to scale the cost into the desired range.

Also logic devices benefit largely from the excellent gate control when implemented in a nanowire structure. However, for viable applications additional requirements have to be fulfilled. Thus, alternative concepts to the conventional MOSFET have emerged. The most important of these are illustrated in Fig. 1.7. With ever decreasing device dimensions doping becomes more and more problematic. On the one side the doping profiles need to be controlled much more precisely. However, due to diffusion during dopant activation an ideal step like profile is hard to achieve even if very short millisecond annealing is used. Second,
the number of dopants in the active channel region decreases. Since the relative variability will scale with $N^{-1/2}$ doping fluctuations will make the control of the threshold voltage nearly impossible. In addition to these difficulties, it has been proven by calculations and experiments, that for certain nanowire geometries, the ionization energies of dopants are higher than in bulk. For nanowires without a surrounding gate dopant deactivation takes place, i.e. to achieve the same doping effect, a higher dopant concentration is needed, especially for thin nanowire diameters.

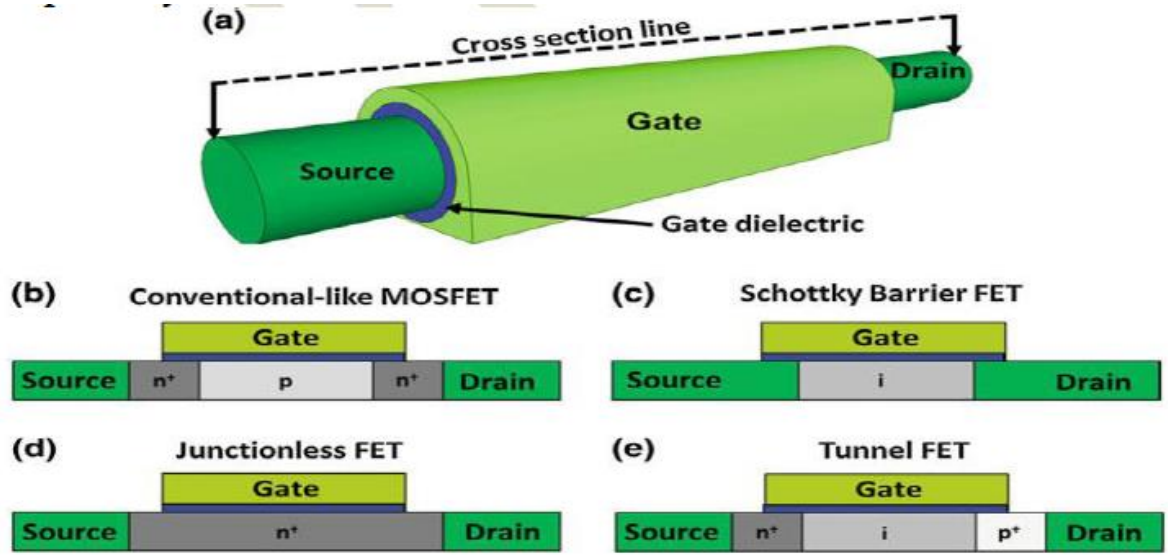


Fig. 1.7 Different options for electron devices using silicon nanowires.

The top drawing a shows a generic 3-D view of a silicon nanowire device with metallic source/drain regions and the surrounding gate. The cross sections b–e illustrates different device concepts: b Conventional nanowire MOSFET, c Schottky Barrier FET, d Junctionless FET and e Tunnel FET.

There are two more aspects that make the use of nanowires in such devices very attractive. First, it is much easier to combine different semiconductors with considerable lattice mismatch in nanowires. Second, nanowire devices can be constructed both in a horizontal and vertical arrangement. Both features have been exploited in where CMOS compatible nanowire structures using a Si/InAs heterostructure as a building block for TFETs are demonstrated.

In the electrostatic doping approach, shown in Fig. 1.8a, the backgate is used as program gate to select electron or hole transport. The program gate bends the silicon bands at both junctions simultaneously. Negative program gate voltages increase the barrier height at the conduction band and thereby block electrons.

In the approach sketched in Fig. 1.8b, the two outer top gates are kept at the same potential and provide a similar function as the back gate in Fig. 1.8a. Thus, this concept allows the individual control of different devices in one chip. In the top-down realization a surrounding gate architecture is provided for both control and program gates.

The RFET device shown in Fig. 1.8c uses two independent top gates each overlapping one of the Schottky junctions. One of them is used to control the polarity. The other is used to control the amount of current flowing through the device. In contrast to the other polarity control concepts and to conventional CMOS, the main part of the active region is ungated.

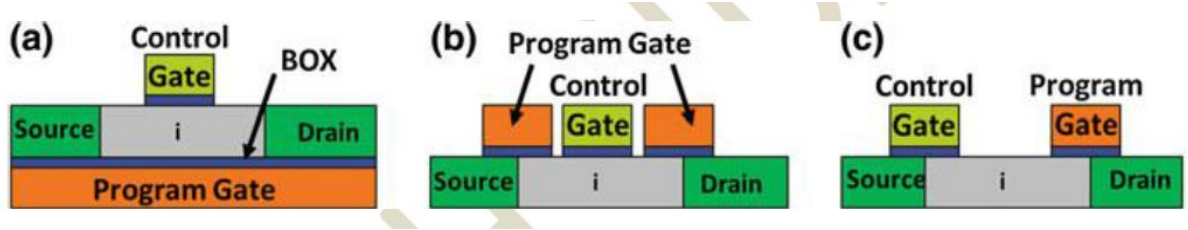


Fig. 1.8 Schematic cross sections of the different concepts for reconfigurable silicon nanowire devices. In the electrostatic doping device (a) the back gate is used to adjust the barrier heights and a top gate controls the current trough the device. The simultaneous control of both Schottky barriers (b) can also be accomplished by using top gates and an additional control gate in the middle then controls the carrier flow. In the RFET (c) approach the program gate above the drain

junction and the control gate above the source junction control the polarity and the current flow respectively

Silicon Nanowire Based Sensors

Generally speaking, a sensor device transforms a physical or chemical signal of the environment into an electrical signal. Normally, the sensor device can be split into the active sensing part, which translates the input signal into an intermediate signal and the transducer that translates the intermediate signal into the final electrical signal. In many cases, the two parts are closely linked. The quasi 1-D properties of nanowires can be utilized in transducers and in some cases also for the active sensing part of the chain. Especially chemical and biochemical sensor research has intensively utilized silicon nanowires in the last decade. But also mechanical sensors can benefit especially from the very high piezoresistance effect observed in silicon nanowires. For example, accelerators that utilize the piezoresistance effect for transduction can be significantly improved. Moreover, freestanding nanowires can be very good oscillators. Combined with the high piezoresistance this enables new classes of devices. The research on chemical and biochemical sensors is again strongly driven by the exploitation of the extremely high surface to volume ratio combined with excellent mechanical stability. Having in mind that excellent field effect transistor devices can be constructed, it is a natural consequence to apply the idea which Bergveld first explored in 1971 in the ion sensitive field effect transistor (ISFET) to place the impedance conversion in potentiometric devices in direct vicinity of the measurement. Using classical planar devices, derivatives of this idea have been established as transducers for chemical and biochemical sensors. The transfer of these ideas to nanowire-based devices was therefore already demonstrated more than a decade ago. For biochemical sensors the diameter of the nanowires can be as small as the species to be detected. As illustrated in Fig. 1.9. This enables a very high sensitivity of the sensor device even if parallel nanowires are used in order to increase the device current, since the current percolation paths are effectively blocked already by a single molecule per nanowire. However, it is important to point out that nanowire based devices have their specific advantage when it comes to a very sensitive detection in small volumes and therefore can enable biosensors that are not possible using a planar transducer.

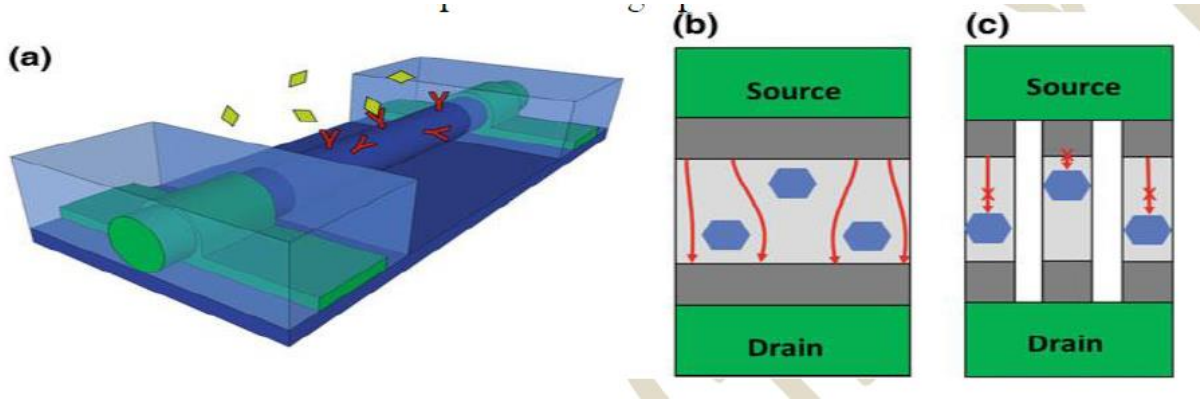


Fig. 1.9 Illustration of a chemical or biochemical sensor based on a nanowire field effect device.a Schematic showing the FET transducer receptors immobilized at the surface. b Top view of a sensor using conventional planar silicon technology. c Top view of nanowire sensor constructed from three parallel nanowires. Red arrows indicate current paths

Silicon Nanowire Based Solar Cells and Anodes for Li-Ion Batteries

Energy generation from renewable sources and storage of electrical energy are among the most pressing technical challenges for our society. These fields can benefit from silicon nanowires as well, as they have the potential to increase the optical absorption and collection efficiency in solar cells. Single nanowire solar cells can be used to study the parameters that influence the

performance of nanowire based photovoltaics. Additionally, they allow a seamless integration with nanowire based electronics and sensors. For doing general purpose solar cells, however, the single wire elements have to be arranged in large arrays. The potential of the single element to enable such a large scale assembly is therefore a strong differentiator for the different concepts. Therefore, the low cost bottom-up growth, which is compatible with different types of substrates, is the fabrication method of choice for such devices. In order to accomplish all the requirements, a coaxial structure is beneficial. First of all, the possibility to fabricate radial pn-junctions has shown promising results. Figure 1.10 shows a schematic view of a silicon nanowire array based solar cell using this concept. Also classical heterojunction concepts using crystalline and amorphous silicon can easily be implemented.

Li-ion batteries are currently one of the best technical solutions to store electrical energy and retrieve it on a short and flexible timescale. Up to date graphite is the standard anode material used in such batteries. However, theoretical calculations predict that silicon can improve the capacity by almost one order of magnitude.

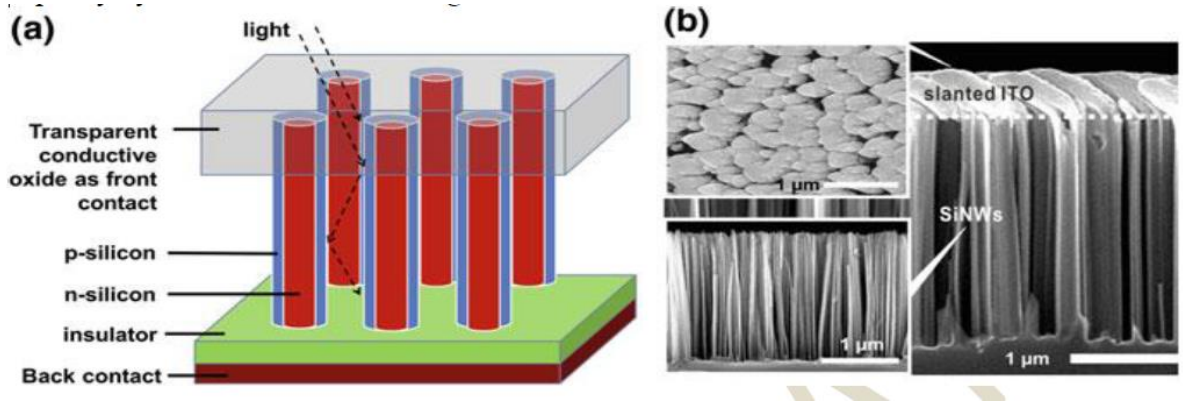


Fig. 1.10a Schematic view of a silicon nanowire based solar cell with a radial pn-junction.
b SEM micrographs from top view and cross section of the solar cell, as well as from the silicon nanowire array.

Carbon Nanotube Transistor Fabrication

INTRODUCTION

Carbon nanotubes (CNTs) are allotropes of carbon with a cylindrical nanostructure. Nanotubes have been constructed with length-to-diameter ratio of up to 132,000,000:1, significantly larger than for any other material. These cylindrical carbon molecules have unusual properties, which are valuable for nanotechnology, electronics, optics and other fields of materials science and technology. In particular, owing to their extraordinary thermal conductivity and mechanical and electrical properties, carbon nanotubes find applications as additives to various structural materials. For instance, nanotubes form a tiny portion of the material(s) in some (primarily carbon fiber) baseball bats, golf clubs, car parts or damascus steel.

Single-wall carbon nanotubes (CNTs) have a large intrinsic mobility and are expected to be useful as a new electronic material. However, their electronic structures depend on their diameters and chirality, where one-third of the pristine CNTs are metallic (*m*-) and the other two-thirds are semiconducting (*s*-),thus, they intrinsically contain metallic contamination. Therefore, it is crucial to mitigate the effect of *m*-CNTs when making use of CNTs as semiconducting materials. There are two approaches, increasing *s*-CNT purity and decreasing the influence of *m*-CNT. Using a CNT random network as a thin film transistor (TFT) channel is one of the best ideas to prevent device shorts caused by *m*-CNTs. According to the simulation work, a CNT random network is tolerant to *m*-CNT contamination. Furthermore, CNT random networks are compatible with solution processes such as *s*-CNT purification and printing fabrication. The device yield and performance of a CNT random network TFT can be increased by the use of purified *s*-CNTs.

On the other hand, printed electronics enable large-area and flexible electronics on plastic substrates .The key feature of print fabrication is simultaneous material deposition, and pattern definition by fully additive processes. This feature reduces the number of process steps and the amount of waste material during fabrication, and leads to low-cost and eco-friendly fabrication from a minimum of materials. Furthermore, maskless printing enables on-demand production by decreasing the lead time with offering flexibility in the circuit design. Therefore, printed electronics are attractive even though the resolution of the printing methods is three orders of magnitude larger than that of photolithography. Actually, it is difficult to fabricate high-density and high-functioning circuits by printing. Therefore, printed electronics are rather suited to implementing devices such as large-area sensing sheets, lightweight human interfaces, RF devices with multiple antennas, and so on.It is expected that such de novo electronics fields will be open by printed electronics.

The key issue is successful fabrication of printed TFTs in order to realize printed electronics, and the performance of the TFTs strongly affects the application field. The performance of printed TFTs is expected to increase by adopting CNT channels with high carrier mobility. A high-mobility TFT with a solution-processed CNT network was fabricated on an Si wafer [8].It showed the excellent potential of a CNT network channel, but it was solid and its gate electrode was not individually fashioned. A flexible and high-mobility TFT was also fabricated on a polymeric substrate [9]; however, it required an additional patterning process for device separation. Inkjet printing is a promising candidate for the direct formation of a CNT network, but because the performance of the current TFTs does not appear competitive [10,11], technological development for printed CNT–TFTs is desired.

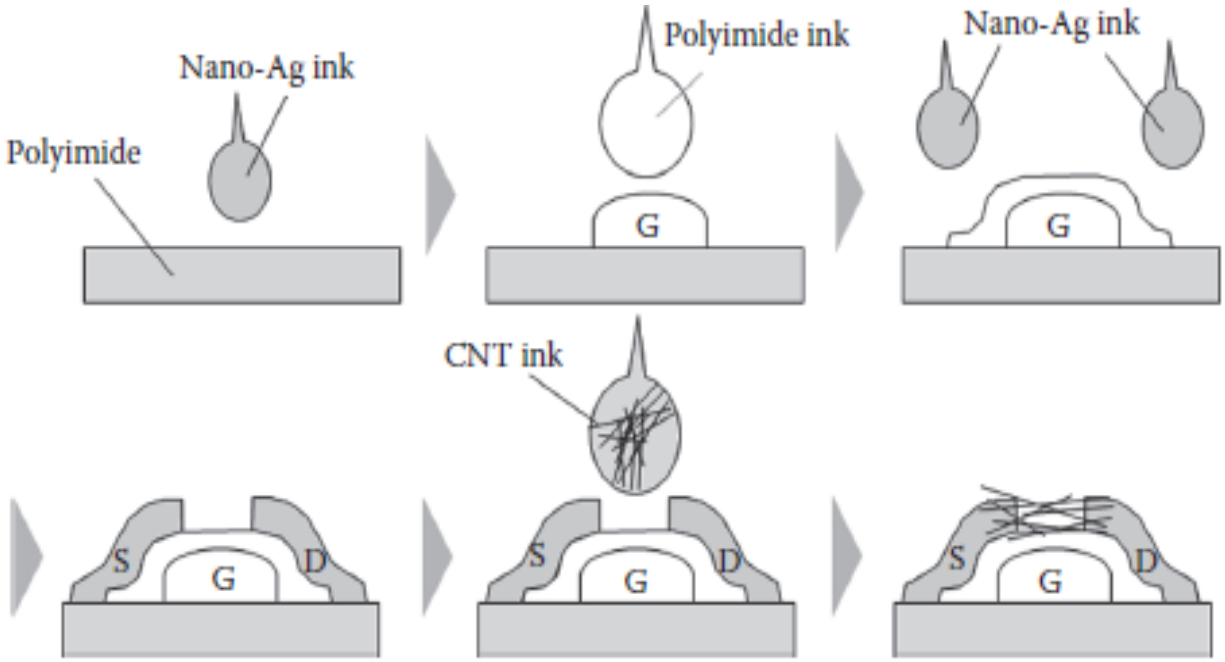
We developed a fabrication technology for printed CNT–TFTs. All electrodes, insulators, and CNT channels were directly printed without additional patterning processes. In this fabrication, surface-free energy was controlled for precise pattern definition. In addition, a mechanism for adsorbing CNTs was applied to channel formation in order to achieve homogeneous dispersion of the CNT random networks. We also developed an *s*-CNT purification method and fabricated the CNT–TFTs on the plastic films. The TFT characteristics clearly demonstrated the advantages of the purified *s*-CNT ink. The on-current of the printed CNT–TFT was increased without deterioration in the on/off ratio. A large field-effect mobility of 3.6 cm2/Vs was obtained for the printed CNT–TFTs with an on/off ratio of about 1000.

PRINTING FABRICATION TECHNOLOGY

Device FabricationFlow

Device fabrication flow is shown in Figure 41.3.All device elements were patterned by maskless printing methods with a minimum of materials.

- First, gate electrodes were printed on a polyimide (PI) film by use of an inkjet printer with nano-Ag ink (NPS-J, Harima Chemicals) and sintered in air.
- Next, gate insulators were formed by an ink dispenser with PI ink (CT4112, Kyocera Chemical)



Print fabrication flow.

In this fabrication process, all device geometries were defined by printing methods without an additional patterning process. Therefore, it is important to control the wettability between the material inks and the underlying surfaces.
In addition, there are two keys in the fabrication process. One is the reliability and uniformity of the printed gate insulators in order to successfully form such layered device structures. The other is the homogeneous dispersion of the CNT networks to improve device quality and performance.

Carbon Nanotube Applications

Since their discovery, many applications have been proposed for vertically aligned carbon nanotubes (CNT).Some potential areas for the use of CNT are Super capacitors, microelectromechanical systems (MEMS), and displays. For these applications, the unique high-aspect-ratio (HAR) features of CNT and their large surface area compared to their volume can be exploited.

One promising application within microelectronics that has received a lot of attention is the use of aligned CNT as vertical interconnects.

CNT are attractive for interconnects as the currently used interconnect materials like Cu are approaching their physical limitations due to the continued downscaling in the semiconductor manufacturing process.

In the roadmap for the semiconductor industry made by the International Technology Roadmap for Semiconductors (ITRS), it can be found that around 2015, for the highest-performance integrated circuits, the electrical current density in the interconnects surpasses the maximum current density of Cu, with no manufacturable known solutions available.CNT, on the other hand, have been demonstrated to be able to carry current densities up to 109 A/cm2.

CNT have been demonstrated to be able to transport heat very efficiently, with thermal conductivities up to 3500 W/mK being demonstrated at room temperature (in comparison, the thermal conductivity of Cu is about 343 W/mK).This could aid in decreasing the temperature of the interconnect stack, again aiding in improving reliability.

Besides the clear reliability advantage, several other issues exist within the interconnect technology.For local interconnects, which form the connections between logic blocks like adders, the interconnect sizes are being scaled with the same trend as the transistor size.Owing to this, the cross section of the interconnect has been pushed well into the nanometer regime.Due to grain boundary and surface scattering, the resistivity of Cu increases by 2–5 times the bulk value.This effect becomes more severe when the interconnect size is further reduced.**Owing to their one-dimensional (1D) nature, CNT do not suffer from these scaling effects**.

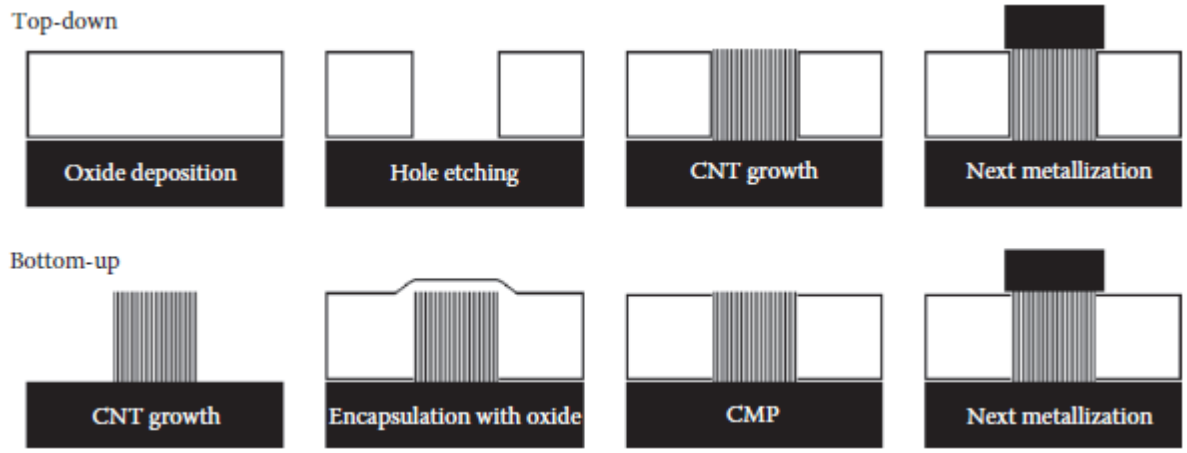
Disadvatages

1D nature does introduce a quantum resistance of 6.45 kΩ per single-walled nanotube (SWCNT), while the situation is slightly more complex for multiwalled nanotubes (MWCNT).This basically means that many parallel conducting tubes are required to achieve an electrical conductivity close to copper. Simulations have shown that dense, vertically aligned SWCNT bundles can indeed compete with Cu vias, while dense MWCNT bundles display a higher resistance. Still, as via resistance is only a small part of the total interconnect resistance, a small increase can be acceptable if other properties like electrical reliability are superior to that of Cu.

For vertical interconnects (vias), a key requirement is thus selective growth of vertically aligned CNT directly on top of electrically conductive layers with high tube density. Two approaches can be defined to integrate interconnects: the traditional top-down approach and the bottom-up approach as presented by Li et al.Both methods are shown in Figure.In the top-down approach, a contact opening is etched using a plasma through the dielectric between the metal layers, followed by CNT growth inside the opening and subsequent metallization.In case CNT density is low and/or the CNT height is longer than the oxide thickness, planarization might be required.

In case of the bottom-up approach, CNT bundles are first grown at the desired location, covered by a dielectric, planarized, and finally covered by the next metallization.The distinct

advantage of the bottom-up method is that it allows the creation of HAR vias, without the need for the etching of, and metal deposition in, HAR openings.The bottom-up approach is also attractive for HAR MEMS.



Graphical representation of top-down and bottom-up integration process.