Sources of Power Dissipation in digital CMOS circuits

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- Low power design considerations :- / Explain various sources of power dissipation in digital CMOS ckts & explain the mtds to reduce p.d.

Ans:- 1. The overall power dissipation P of the chip is very important in modern VLSI designs.

2. If a battery power supply is used, the P determines the operating time before a recharge is needed.

3. Low-power design techniques have been developed at both the ckt & system level.

There are three main sources of p.d in a digital CMOS ckt.

1. DC power P_{DC} that is due to direct conduction paths from V_{DD} to gnd when i/ps are stable. leakage currents are the main cause in standard static CMOS ckts.

2. Switching power P_{sw} that is dissipated when an i/p change causes the power supply to have direct current flow path to ground through the Trs.

3. Dynamic switching power P_{dyn} due to charging and discharging capacitive nodes.

Dynamic switching power is estimated from the equation below

$$P_{dyn} = \alpha C V^2 f$$

where, C is the switching capacitances in farads, α is the activity factor, V is the voltage swing, and f is the signal freq^n.

- The instantaneous total p.d is

$$P = P_{DC} + P_{sw} + P_{dyn}$$

1. Considering first DC leakage term ie

$$P_{DC} = I_{DDQ} V_{DD}$$

where I_{DDQ} is the quiescent leakage current that flows when i/ps are not changing.
The value of leakage current for a Tr is process dependent. The total I_{DDQ} for the chip ↑ses with no of Trs & also depends upon the ckt design technique.
- Static CMOS logic gates exhibits smallest I_{DDQ} usually less than 10μA

2. Switching power Psw is a consequence of a gate i/p s/g transition causing a direct current flow path from V_{DD} to grd

$$P_{sw} = I_{sw} V_{DD}$$

where I_{sw} is the average DC current flow.

3. The dynamic p.d is usually considered to be most difficult to deal with

$$P_{dyn} = \alpha C V^2 f$$

The above expression shows that P_{dyn} ↑ses proportionately with the s/g switching freqn f.
One approach to ↓se P_{dyn} is to reduce the power supply vtg V_{DD}
Processor core vtgs are currently below 2V or even lower operating vtgs.
A reduced power supply vtg is also advantageous in battery-operated units.

$$I_D = \frac{\beta}{2}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right]$$

Since the highest vtg in the ckt is V_{DD}, reducing it implies that I_D will also ↓se.
Reducing I_D implies that it will take longer to charge the o/p cap, ↑sing both the rise & fall time. This slows down the gate switching speed. To compensate for this effect, we can ↑se the device

transconductance term

$$\boxed{\beta = \mu_n C_{ox} \left(\frac{W}{L}\right)}$$

Since,

$$\boxed{C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}} \rightarrow \text{Gate oxide Cap}$$

Shrinking the gate oxide thickness t_{ox}, ↑ses β so improved processing helps. Otherwise, we must ↑se the channel width W to maintain the speed.