4.5 THE SWITCHED CAPACITOR

The filters investigated so far, known as *continuous-time filters*, are characterized by the fact that H_0 and Q are usually controlled by component ratios and ω_0 is controlled by component products. Though ratios can easily be maintained with temperature and time by using devices with adequate tracking capabilities, products are inherently more difficult to control. Moreover, IC processes do not lend themselves to the fabrication of resistances and capacitances with the magnitudes (10^3 to 10^6 Ω and 10^{-9} to 10^{-6} F) and accuracies (1% or better) typically required in audio and instrumentation applications.

If filter functions are to coexist with digital functions on the same chip, filters must be realized with the components that are most natural to VLSI processes, namely, MOS transistors and small MOS capacitors. This constraint has led to the development of switched-capacitor (SC) filters,[10-12] which simulate resistors by periodically operating MOS capacitors with MOSFET switches, and produce time constants that depend on capacitance ratios rather than R-C products.

To illustrate, let us start with the basic MOSFET-capacitor arrangement of Fig. 4.23*a*. The transistors are n-channel enhancement types, characterized by a low channel resistance (typically $<10^3$ Ω) when the gate voltage is high, and a high resistance (typically $>10^{12}$ Ω) when the gate voltage is low. With an off/on ratio this high, a MOSFET can be regarded for all practical purposes as a switch.

If the gates are driven with nonoverlapping out-of-phase clock signals of the type in Fig. 4.23*b*, the transistors will conduct on alternate half cycles, thus providing a single-pole double-throw (SPDT) switch function with break-before-make characteristics.

Referring to the symbolic switch representation of Fig. 4.24*a* and assuming $V_1 > V_2$, we observe that flipping the switch to the left charges C to V_1, and flipping it to the right discharges C to V_2. The net charge transfer from V_1 to V_2 is $\Delta Q = C(V_1 - V_2)$. If the switch is flipped back and forth at a rate of f_{CK} cycles per second, the charge transferred in 1 second from V_1 to V_2 defines an average current

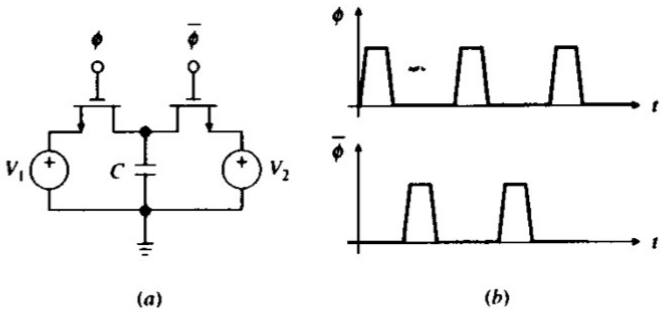

FIGURE 4.23
Switched capacitor using a MOSFET SPDT switch, and clock drive for the MOSFETs.

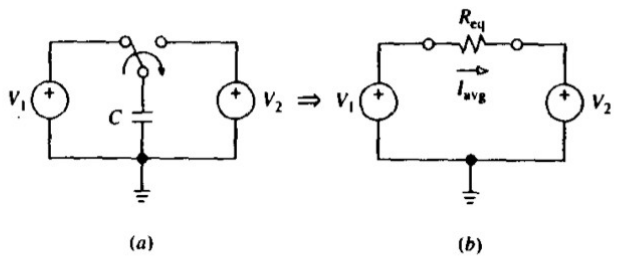

FIGURE 4.24
Resistance simulation using a switched capacitor.

$I_{avg} = f_{CK} \times \Delta Q$, or

$$I_{avg} = C f_{CK}(V_1 - V_2) \tag{4.16}$$

Note that charge is flowing in packets rather than continuously. However, if f_{CK} is made sufficiently higher than the highest-frequency components of V_1 and V_2, the process can be regarded as continuous, and the switch-capacitor combination can be modeled with an equivalent resistance

$$R_{eq} = \frac{V_1 - V_2}{I_{avg}} = \frac{1}{C f_{CK}} \tag{4.17}$$

The model is depicted in Fig. 4.24*b*. Let us investigate how such a resistance can be used to implement, what by now has proved to be the workhorse of active filters, namely, the integrator.

SC Integrators

As we know, the *RC* integrator of Fig. 4.25*a* yields $H(j\omega) = -1/(j\omega/\omega_0)$, where the unity-gain frequency is given by

$$\omega_0 = \frac{1}{R_1 C_2} \tag{4.18}$$

Replacing R_1 by an SC resistance gives the SC integrator of Fig. 4.25*b*. If the input frequency ω is such that

$$\omega \ll \omega_{CK} \tag{4.19}$$

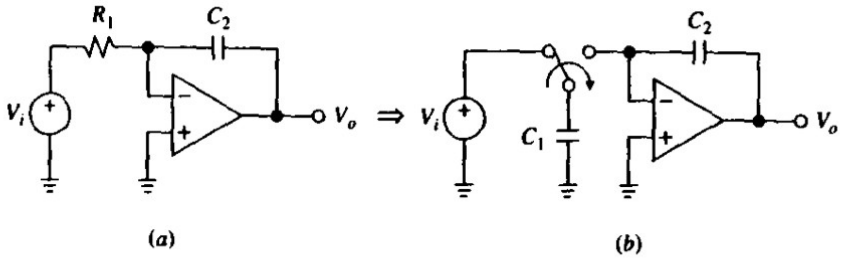

FIGURE 4.25
Converting an *RC* integrator to an SC integrator.

where $\omega_{CK} = 2\pi f_{CK}$, then current flow from V_i to the summing node can be regarded as continuous, and ω_0 is found by substituting R_{eq} into Eq. (4.18),

$$\omega_0 = \frac{C_1}{C_2} f_{CK} \tag{4.20}$$

This expression reveals three important features that hold for SC filters in general, not just for SC integrators:

1. There are no resistors. This is highly desirable from the viewpoint of IC fabrication, since monolithic resistors are plagued by large tolerances and thermal drift, and also take up precious chip area. Switches, on the other hand, are implemented with MOSFETs, which are the basic ingredients of VLSI technology and occupy very little chip area.
2. The characteristic frequency ω_0 depends on capacitance ratios, which are much easier to control and maintain with temperature and time than R-C products. With present technology, ratio tolerances as low as 0.1% are readily achievable.
3. The characteristic frequency ω_0 is proportional to the clock frequency f_{CK}, indicating that SC filters are inherently of the programmable type. Varying f_{CK} will shift the response up or down the frequency spectrum. If, on the other hand, a fixed and stable characteristic frequency is desired, f_{CK} can be generated with a quartz crystal oscillator.

Equation (4.20) also shows that by judicious choice of the values of f_{CK} and the C_1/C_2 ratio, it is possible to avoid undesirably large capacitances even when low values of ω_0 are desired. For instance, with $f_{CK} = 1$ kHz, $C_1 = 1$ pF, and $C_2 = 15.9$ pF, the SC integrator gives $f_0 = (1/2\pi)(1/15.9)10^3 = 10$ Hz. An RC integrator with the

the SC integrator gives $f_0 = (1/2\pi)(1/15.9)10^3 = 10$ Hz. An RC integrator with the same f_0 could be implemented, for instance, with $R_1 = 1.59$ MΩ and $C_2 = 10$ nF. Fabricating these components monolithically and maintaining the value of their product within 0.1% would be unrealistic. Current SC filters use capacitances in the range of 0.1 pF to 100 pF, with the 1-pF to 10-pF range being the most common. The upper limit is dictated by die area considerations, and the lower limit by parasitic capacitances of the SC structure.

To minimize the effect of parasitic capacitances and also increase circuit versatility, practical SC integrators are implemented with SPDT switch pairs, in the manner of Fig. 4.26. In Fig. 4.26*a*, flipping the switches down discharges C_1 to zero, and flipping the switches up charges C_1 to V_i. Current will thus flow into the summing junction of the op amp if $V_i > 0$, and out if $V_i < 0$, indicating that the integrator is of the inverting type.

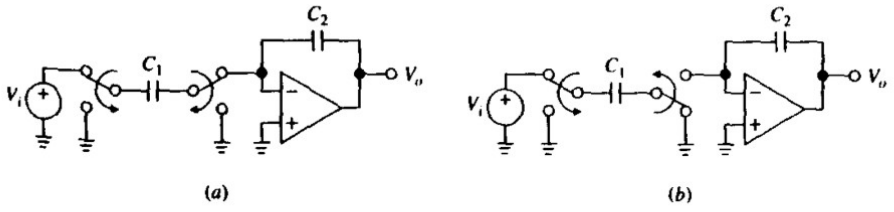

FIGURE 4.26
Inverting and noninverting SC integrators.

Changing the phase of one of the switches yields the circuit of Fig. 4.26*b*. With the switches in the positions shown, the left plate of C_1 is at V_i and the right plate at 0 V. Commutating both switches will discharge C_1 to 0 V, thus pulling charge out of the summing junction if $V_i > 0$, and pushing current into the junction if $V_i < 0$. A simple phase rewiring of the two MOSFETs making up one of the switches inverts the direction of I_{avg}, resulting in an SC integrator of the noninverting type. We shall exploit the availability of this type of integrator in the next sections.

Practical Limitations of SC Filters

There are some important limitations that we need be aware of when applying SC filters.[10] First, there are limits on the permissible range of f_{CK}. The upper limit is dictated by the quality of the MOS switches and the speed of the op amps. Taking 10 pF as a typical switched capacitance and 1 kΩ as a typical resistance of a closed MOS switch, we observe that the time constant is on the order of $10^3 \times 10^{-11} = 10$ ns. Considering that to charge a capacitance to within 0.1% of its final voltage takes about seven time constants ($e^{-7} \cong 10^{-3}$), it follows that the minimum time interval between consecutive switch commutations is on the order of 10^2 ns. This also happens to be the typical time it takes for the step response of a MOS op amp to settle within 0.1% of its final value. Consequently, the upper limit for f_{CK} is in the megahertz range.

The lower practical limit for f_{CK} is dictated by the leakage of open MOS switches and the input bias currents of op amps, both of which tend to discharge the capacitors and, hence, to destroy the accumulated information. At room temperature these currents are in the picoampere range. Assuming a maximum acceptable droop of 1 mV across a capacitor of 10 pF, we have $f_{CK} \geq (1 \text{ pA})/[(10 \text{ pF}) \times (1 \text{ mV})] = 10^2$ Hz. In summary, the permissible clock range is typically $10^2 \text{ Hz} < f_{CK} < 10^6 \text{ Hz}$.